Macintosh®

Macintosh IIci

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Chapter 1 **Introduction**

The Apple Macintosh IIci is a new offering in the Macintosh family of computers. It brings with it a history of compatibility, as well as new features. These old and new features are described in this chapter.

Features

The Macintosh IIci is the first in a new series of Macintosh computers compatible with the Macintosh II family (Macintosh II, Macintosh IIx, and Macintosh IIcx), and offering improved performance and flexibility. The new architecture is based upon the Memory Decode Unit (MDU) and RAM-based video chips (RBV). Key new features are a 25 MHz clock speed and on-board video; most other features are the same as the Macintosh IIcx.

The major new features of the design are:

- MDU/RBV Architecture — A new chip set provides memory decoding and low-cost video by utilizing existing on-board DRAM for the frame buffer.
- 25 MHz clock speed — Faster clock speed for improved performance.
- On board video — On-board video support for 12″ B&W, 13″ RGB, and 15″ B&W Portrait monitors.
- Burst reads — Burst reads from RAM.
- DRAM Parity — Optional DRAM parity generation and detection, when 9-bit DRAM SIMMs and a Parity-Generator Chip (PGC) are installed.
- Cache Connector — An optional memory cache card.

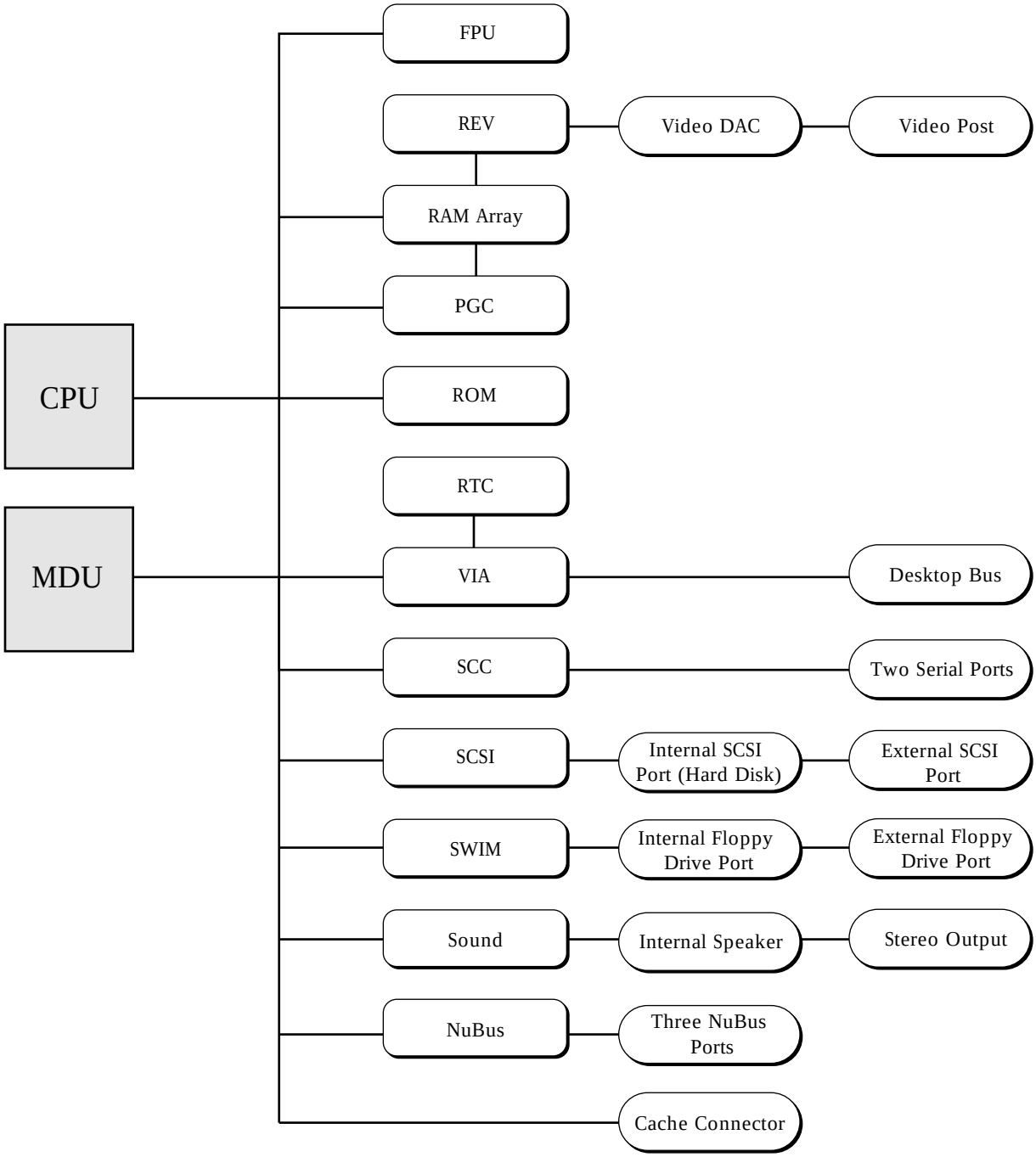
Additional features that separate the Macintosh IIci from the Macintosh II/IIx/IIcx are:

- RAM Expansion — Address space for up to 128 MB of RAM on the motherboard. 4 Mbit DRAM is now supported (and 16 Mbit if it remains compatible with the 4 Mbit DRAM). Over 800 MB of expansion RAM is possible in NuBus slots.
- ROM Expansion — A ROM SIMM allows future ROM revision in the field.

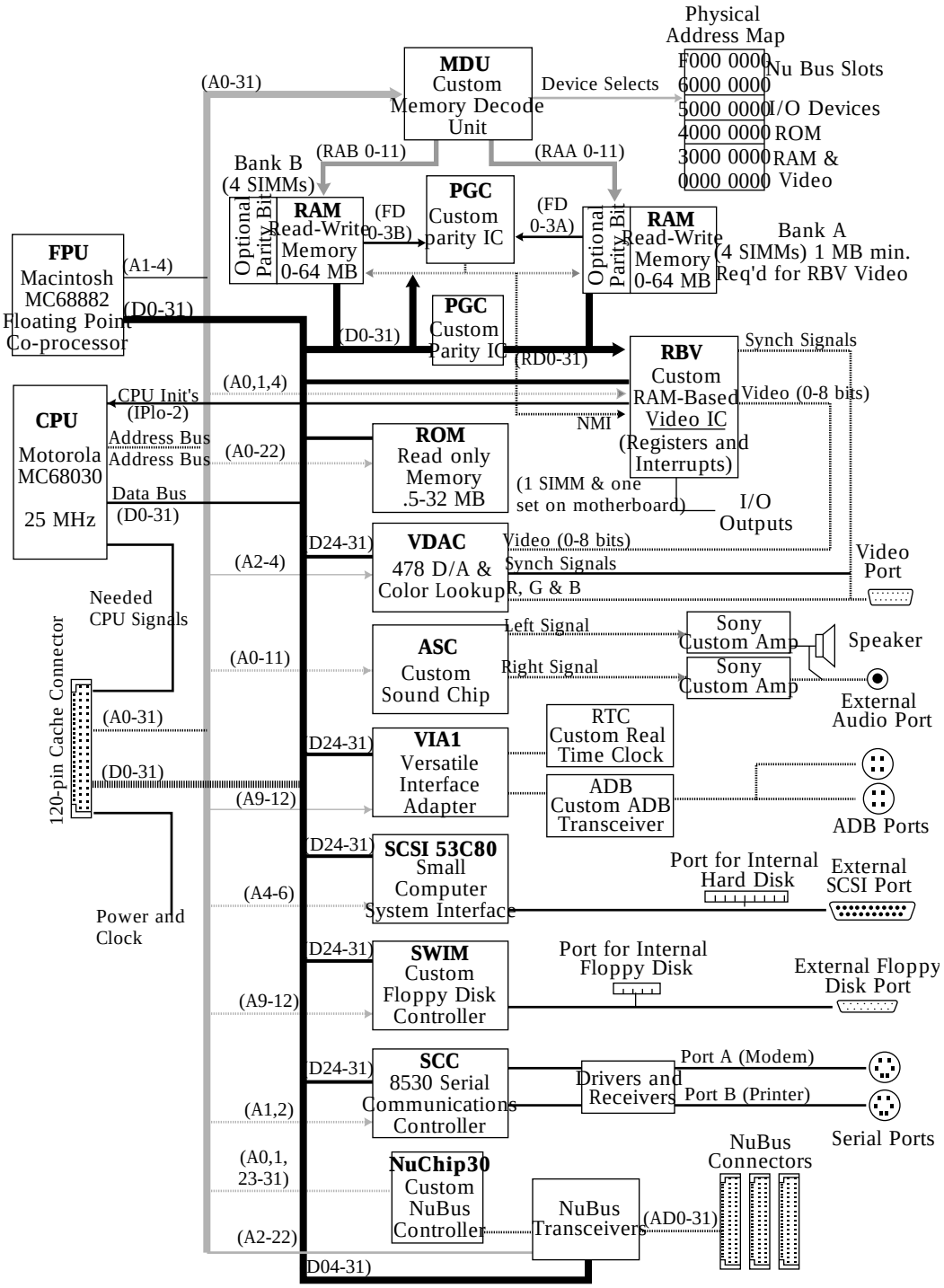
- Slot Expansion — Three NuBus expansion slots which allow full size cards (13″ x 4″). Slots support full 32 bit address and data.
- Hard Drive support — Room for one internal 3 1/2″ hard drive with SCSI interface. Additional storage capacity through up to 6 additional external drives connected to SCSI port on back of CPU.
- Floppy Drive support — One internal 1.4 MB Sony 3.5″ floppy drive. Support for one external 800K or 1.4 MB Sony 3.5″ floppy drive. *(see Compatibility)*
- 68030 Processor — True 32-bit processor running at 25 MHz for high performance. The 68030 has internal 256-byte data and instruction caches as well as on-chip memory management. Burst reads to the on-chip cache are supported. The 68030 is compatible with existing Macintosh timings and software.
- Memory Management — True 32-bit address translation with hardware page replacement.
- Built-in Serial Ports — Two Macintosh 8-pin serial ports supporting RS–232, RS–422 and AppleTalk.
- ADB (Apple Desktop Bus) — Apple Desktop Bus allows additional input devices (e.g. graphics tablet) to be added at any time. Keyboard and mouse are standard input devices.
- Numerics Processor — The 25 MHz 68882 Floating-Point Coprocessor Unit (FPU) allows high-speed, high-accuracy floating-point computation to IEEE standards.
- Soft Power Control — Keyboard power-on and software power-off help ensure data integrity on disks. Slot access to power control allows power to be controlled by NuBus cards. The mechanical on/off button can be locked in the *on* position so the computer will automatically turn back on after an A/C power outage.
- Real Time Clock — Macintosh-compatible clock and parameter RAM with 7-year battery protection.

• Sound	Apple sound chip provides Macintosh-compatible sound and four-voice synthesis in hardware.
• Video	On-board video support for the Apple 12-inch B&W, 13-inch RGB, and 15-inch B&W Portrait monitors. NuBus video-card options are also available.

- **Figure 1-1** System block diagram



- **Figure 1-2** Hardware block diagram



Compatibility

Disks

The external floppy drive port on this product does not support the 400K floppy drive. It does support 400K disks used in the 800K drive.

Memory

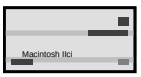
Physical memory is not contiguous, as it is on the Macintosh II, IIx, and IIcx. The 68030 on-chip MMU is used to join the discontiguous blocks of physical memory to present contiguous logical memory to application software. RAM must be 80 ns access time (or faster), fast page mode. For additional RAM specifications, see see Chapter 3, "The RAM Interface."

History of the Macintosh II Family

The Macintosh IIci continues the modular design center. Macintosh IIcx began this evolution by taking the Macintosh IIx and removing three NuBus slots and a floppy-disk drive. Most other changes from the Macintosh IIx were in appearance, and Apple's official approval (and encouragement, even) to stand it up on end. The box was redesigned, the power supply and power-on circuitry redesigned, and the hard-disk drive was changed from 5 1/2" to 3 1/2".

The Macintosh IIci project continues this evolution with a completely new architecture, built around the Memory Decode Unit (MDU) and RAM Based Video (RBV) chips. The NuChip was also modified, becoming the NuChip30, to work efficiently with the 68030 bus.

- **Table 1-1** System comparisons

	Macintosh II	Macintosh IIx	Macintosh IIcx	Macintosh IIci
				
processor	16 MHz 68020	16 MHz 68030	16 MHz 68030	25 MHz 68030
coprocessor	16 MHz 68881	16 MHz 68882	16 MHz 68882	25 MHz 68882
NuBus	6 NuBus Slots	6 NuBus Slots	3 NuBus Slots	3 NuBus Slots
Other	*none*	*none*	*none*	Cache Connector
architecture	GluChip/NuChip	GluChip/NuChip	GluChip/NuChip	MDU/RBV/NuChip30
Parity	*none*	*none*	*none*	optional PGC
int. floppy	2 internal floppies	2 internal floppies	1 internal floppy	1 internal floppy
ext. floppy	no external floppy	no external floppy	1 external floppy	1 external floppy
hard drive	internal 5 1/4″ or 3 1/2″ hard drive	internal 5 1/4″ or 3 1/2″ hard drive	internal 3 1/2″ hard drive	internal 3 1/2″ hard drive
ROM socket	DIP	SIMM	DIP & SIMM	DIP & SIMM
ROM speed	150 ns	150 ns	150 ns	150 ns
RAM speed	120 ns	120 ns	120 ns	80 ns fast page mode

References

Additional information relating to this design can be found in the following documents.

- MC68030 Enhanced 32-Bit Microprocessor User's Manual, Second Edition, Motorola, MC68030UM/AD REV 1, 1989.
- MC68882 Floating-Point Coprocessor User's Manual, Motorola, Prentice-Hall, 1985.
- NuBus Specification (Draft 1.1), NuBus Subcommittee, 1985.
- Product Databook, Brooktree, First Edition, 1988
- SCSI Small Computer System Interface, ANSI X3T9.2/82-2 Rev. 17B.

- Controller Products Data Book (VIA), Rockwell, 1987.
- Z8030 Z-BUS SCC/Z8530 SCC Serial Communications Controller, Product Specification, Zilog, September 1986.

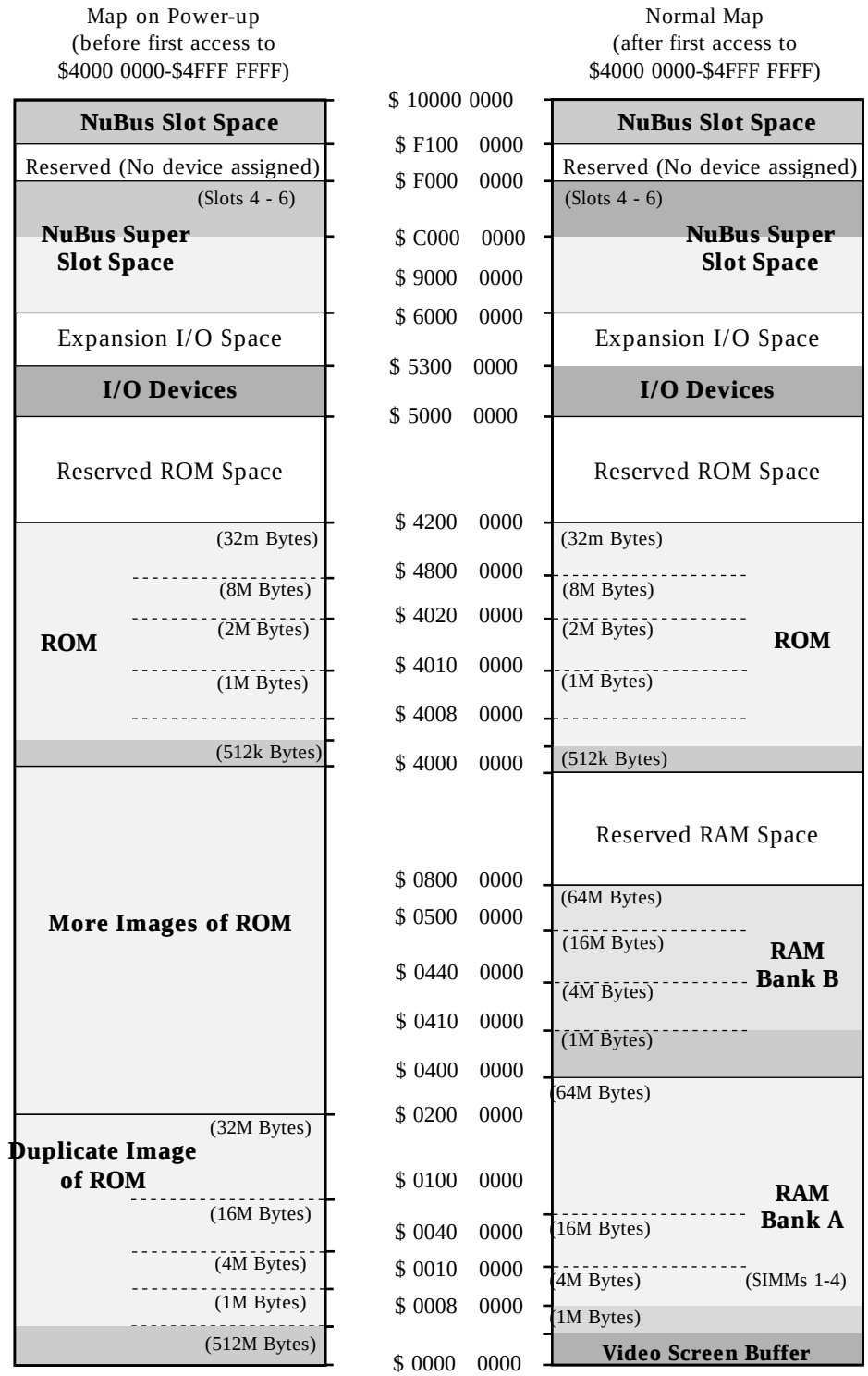
Chapter 2 **Address Mapping**

The Macintosh IIci uses a memory mapping scheme which is implemented by a new custom IC, the Memory Decode Unit. The memory map as controlled by the MDU, is described in this chapter.

Address Space

The address space is decoded by the Memory Decode Unit (MDU). On power up, ROM is mapped by the MDU to physical location $0000 0000. This enables the starting address, retrieved by the 68030 on reset, to be stored in ROM. After the first access to the true ROM address space ($4000 0000 through $4FFF FFFF), the normal memory map is imposed by the MDU. The only change from one map to the other is that in the power-up map ROM is selected for addresses $0000 0000-3FFF FFFF, whereas the normal map selects RAM for that address space as shown in Figure 2-1.

- **Figure 2-1** The physical memory maps



Programmable Memory Management

Memory mapping is performed by the Memory Management Unit (MMU), whose function is built into the MC68030 processor. Having the MMU function built into the microprocessor saves one wait state over the use of an external MC68851 PMMU or Apple HMMU with the MC68020 on the Macintosh II. However, the 68030 on-chip MMU provides only a subset of the 68851's capabilities. The 68030 allows memory management that is required when running virtual memory systems such as A/UX.

Software determines the memory size at power-on and compiles a table describing the current memory configuration. The MMU is then programmed based on this table to provide contiguous logical memory from the potentially non-contiguous physical segments in Banks A and B.

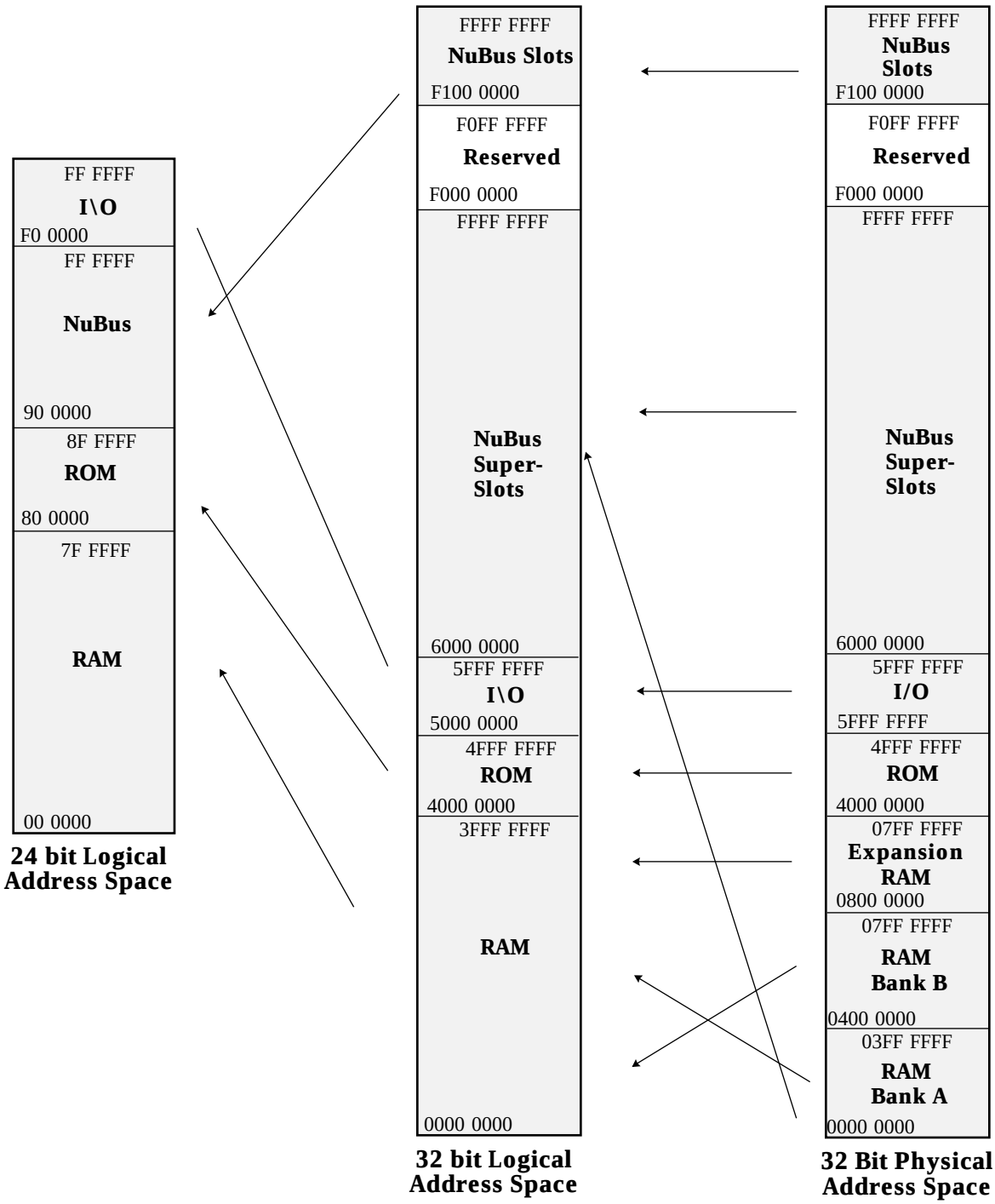
The memory map

The 24/32 bit Memory Map is designed to allow existing Macintosh software to use a 24 bit address mode while new software can use the full 32 bit address space. It is implemented as a simple direct mapping, as shown in Table 2-1 and Figure 2-2. The memory maps are set up by the 68030's on-chip MMU. Note that this memory mapping scheme maps the video frame buffer into the NuBus superslot space.

- **Table 2-1** 24-bit–to–32-bit mapping mode

Usage		24 bit Address Range		32 bit Address Range	
		from	to	from	to
RAM		$xx00 0000	$xx7F FFFF	$0000 0000	$07FF FFFF
ROM		$xx80 0000	$xx8F FFFF	$4000 0000	$400F FFFF
(not on IIci)	NuBus Address $9	$xx90 0000	$xx9F FFFF	$F900 0000	$F90F FFFF
(not on IIci)	NuBus Address $A	$xxA0 0000	$xxAF FFFF	$FA00 0000	$FA0F FFFF
(not on IIci)	NuBus Address $B	$xxB0 0000	$xxBF FFFF	$FB00 0000	$FB0F FFFF
Slot 4	NuBus Address $C	$xxC0 0000	$xxCF FFFF	$FC00 0000	$FC0F FFFF
Slot 5	NuBus Address $D	$xxD0 0000	$xxDF FFFF	$FD00 0000	$FD0F FFFF
Slot 6	NuBus Address $E	$xxE0 0000	$xxEF FFFF	$FE00 0000	$FE0F FFFF
I/O Space		$xxF0 0000	$xxFF FFFF	$5000 0000	$500F FFFF

- **Figure 2-2** 24- and 32-bit address spaces



Chapter 3 **The RAM Interface**

The Macintosh IIci introduces new memory read and write techniques—such as burst reads and parity checking—which are implemented in RAM SIMMS. This chapter details the electrical and physical details of the RAM, as well as the optional Parity Generator Chip for providing memory parity checking. How video makes use of RAM, and RAM refresh are also described in this chapter.

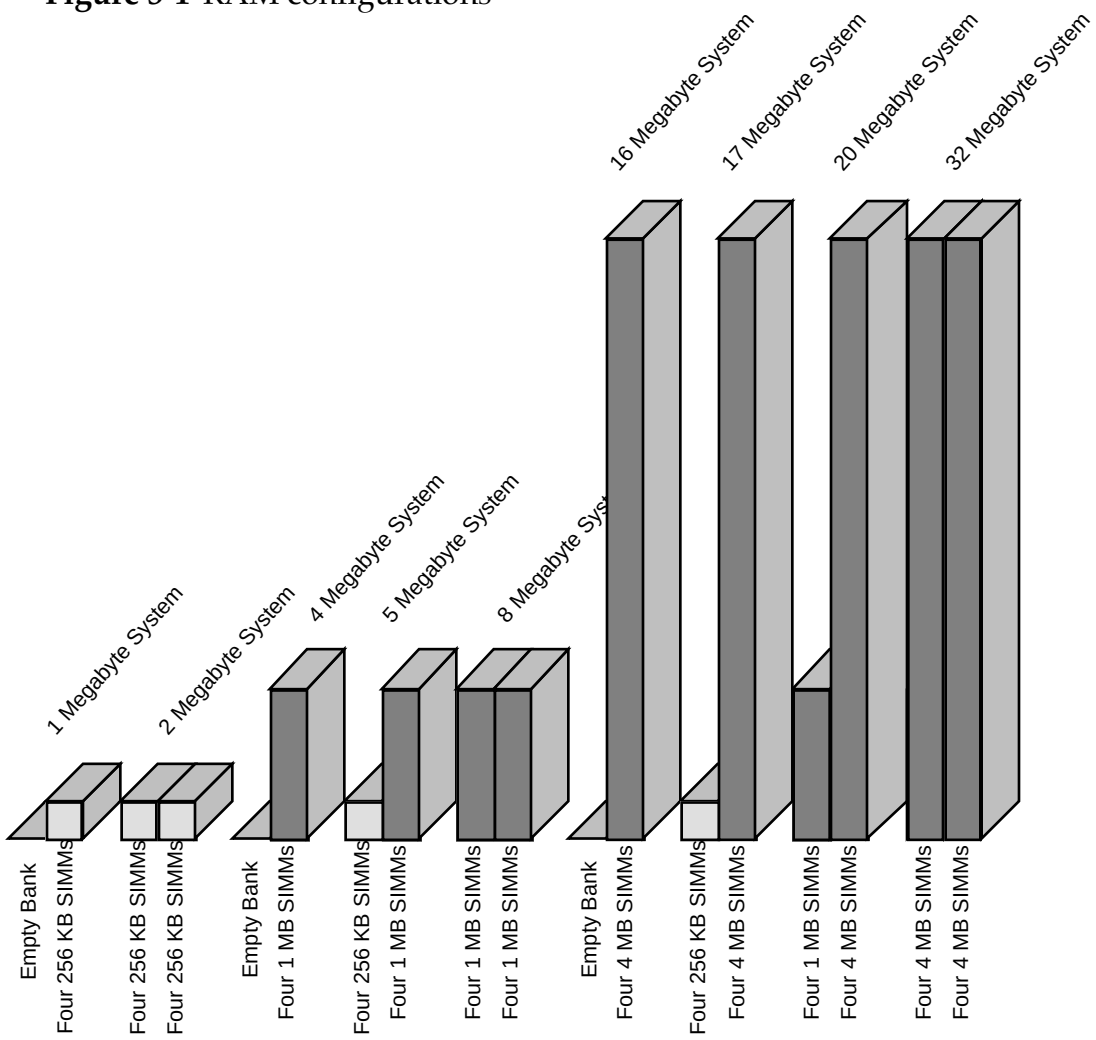
RAM Configuration

The Random Access Memory (RAM) interface on the motherboard is designed to support from 1 MB to 128 MB of RAM. The interface supports burst-read mode which allows a 5 clock initial access followed immediately by three 2 clock accesses. The RAM is mounted in Single Inline Memory Modules (SIMMs) which each contain up to eight or nine Dynamic Random Access Memories (DRAMs) on a PC board. Nine-bit DRAM SIMMs are necessary only if the optional Parity Generator Checker (PGC) is installed and parity checking is desired, but parity checking will be enabled only if all installed SIMMs are 9-bit SIMMs. RAM is divided into two banks, A and B, of four SIMM sockets each. Each bank may contain either no RAM or four 256K SIMMs (made from 1 Mbit fast-page-mode parts), four 1 MB SIMMs, four 4 MB SIMMs, or four 16 MB SIMMs. The amount of motherboard RAM is changed by installing four of the same size SIMMs into either bank. (See Figure 3-1). Bank A must have DRAM installed in order to use on-board video.

Note that although the Macintosh IIci supports parity checking, the standard machine configuration will be shipped with eight-bit DRAM SIMMs. For parity, special units with the PGC and nine-bit DRAM SIMMs must be ordered.

Each bank of RAM is decoded into one of two fixed contiguous 64 MB address spaces. Since these banks are at fixed physical locations (*see Physical Memory Map*), the overall RAM address space will not be contiguous unless Bank A is full (16 Mbit DRAM parts). Bank A occupies physical address $0000 0000 to $03FF FFFF and Bank B occupies physical addresses $0400 0000 to $07FF FFFF. Unless 16 Mbit DRAMs are used in a bank of memory, some part of the 64 MB address space will be unused. Such space will wrap, containing multiple images of the existing RAM in that bank's address space. For example, if 1 MB of RAM is inserted into Bank A then $0000 0000 to $000F FFFF will contain the normal image and $0001 0000 to $0001 FFFF will contain the second image, and so on, with a total of 63 copies of the normal 1 MB address range. This address wrapping allows the ROM to determine how much memory is present in each bank.

- **Figure 3-1** RAM configurations



NOTES:

1 Banks A and B are interchangeable. For best performance with on-board video, put the smaller SIMMs in bank A.

2 Use of on-board video requires DRAM in bank A.

3 256K SIMMs will be made from 256K x 4 fast page mode DRAM parts (1 MBit technology), unless 256K x 1 fast page mode DRAM parts (256 KBit technology) become more readily available.

Use of RAM by the Video

If the on-board video is used, RAM must be installed in Bank A because the frame buffer is maintained beginning at physical address $0000 0000. The RBV's frame buffer is variable in size, depending on the currently selected bit-depth and on the size of the video monitor plugged in to the on-board video port. The RBV will require only the amount of memory to hold the contents of the screen; no additional memory is used for the frame buffer by the RBV. Software will determine the maximum (default, or previous selection by the user) video bit depth to be made available at startup, and set aside that memory for video. If a smaller bit depth than this maximum is selected by the user, operating system software may make use of this additional space.

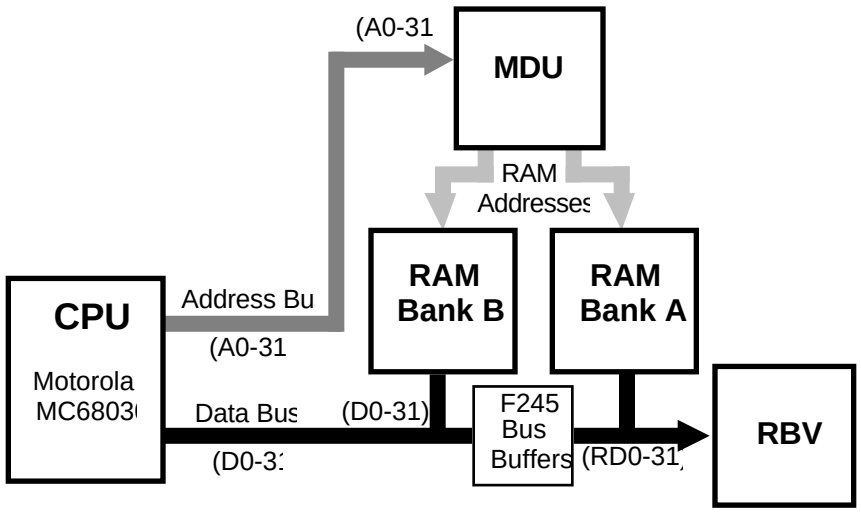
The RBV requests memory in bursts and the MDU passes the data from memory, automatically incrementing a pointer to the current location in the frame buffer. The RBV tells the MDU to reset this pointer at the end of a screen, and the MDU sets the frame buffer pointer back to physical address $0000 0000. (All addresses dealt with by the MDU must be physical because all logical memory mapping is performed by the 68030's on-board MMU.)

The operating system may map this region of memory elsewhere, in order to make it look like any other video device. The operating system decides at startup how much of Bank A to devote to video, and how much may be mapped to the normal RAM address space.

Video accesses affect only Bank A memory access because the data bus between the RAM banks can be disconnected by an F245 buffer as shown in Figure 3-2. This allows the RBV to fetch data from Bank A without interrupting CPU access to Bank B or I/O devices. Each bank of RAM is accessed independently by the MDU, so it can decode addresses for the CPU and the RBV at the same time without interference.

For clarity, only the necessary components are illustrated in Figure 3-2.

- **Figure 3-2** RAM and video block diagram



DRAM Requirements and Refresh

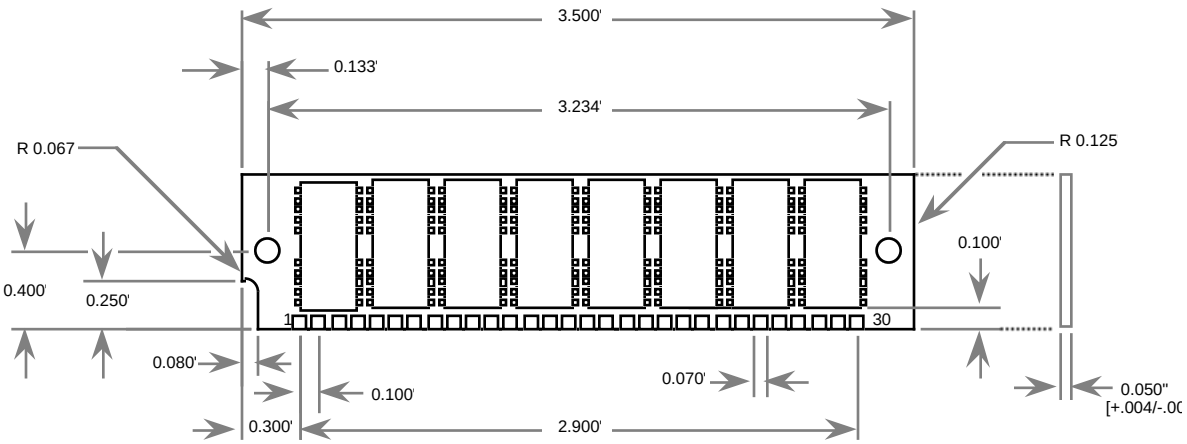
The RAM interface requires 80 ns RAS access time DRAMs with CAS before RAS refresh and fast page mode. The Table 3-1 gives more detailed DRAM specifications. These DRAMs must be mounted on 30 pin SIMMs with bypass capacitors. Table 3-2 and Table 3-3 show the pinout for the SIMMs both with and without parity, and the connections made to the processor bus.

- **Table 3-1** DRAM access time requirements

RAS Access Time	80 ns
CAS Access Time	20 ns
Access Type	Fast Page Mode
Refresh Type	CAS~ before RAS~
Refresh Period	15.6 µs

RAM refresh is performed by the MDU with CAS before RAS cycles. The refresh cycles are six CPU clocks long. Refresh is initiated at the same time in both banks of RAM every 15.6 µs; however, it continues independently in each bank so that if it must be held off until the completion of a CPU or video access in one bank, the other bank's refresh is not also held off. Refresh does not affect the processor at all if the processor is accessing anything except RAM.

- **Figure 3-3** RAM SIMM diagram



- **Table 3-2** Eight-bit DRAM SIMM pinout

Pin #	SIMM Function	Processor Bus Function	Pin #	SIMM Function	Processor Bus Function
1	+5V	+5V	16	DQ4	D4, D12, D20, *or* D28
2	CAS~	CASLL~, CASLM~, CASUM~ *or* CASUU~	17	RA8	$A19_{RAS}$, $A18_{CAS}$
			18	RA9	$A21_{RAS}$, $A20_{CAS}$
3	DQ0	D0, D8, D16, *or* D24	19	RA10	$A23_{RAS}$, $A22_{CAS}$
4	RA0	$A6_{RAS}$, $A2_{CAS}$	20	DQ5	D5, D13, D21, *or* D29
5	RA1	$A7_{RAS}$, $A3_{CAS}$	21	WE~	RAMRW~
6	DQ1	D1, D9, D17, *or* D25	22	+5V	+5V
7	RA2	$A8_{RAS}$, $A4_{CAS}$	23	DQ6	D6, D14, D22, *or* D30
8	RA3	$A9_{RAS}$, $A5_{CAS}$	24	RA11	$A24_{RAS}$, $A25_{CAS}$
9	GND	GND	25	DQ7	D7, D15, D23, *or* D31
10	DQ2	D2, D10, D18, *or* D26	26	NC	NC
11	RA4	$A11_{RAS}$, $A10_{CAS}$	27	RAS~	RAS0~ *or* RAS1~
12	RA5	$A13_{RAS}$, $A12_{CAS}$	28	NC	Pullup to +5V
13	DQ3	D3, D11, D19, *or* D27	29	NC	NC
14	RA6	$A15_{RAS}$, $A14_{CAS}$	30	+5V	+5V
15	RA7	$A17_{RAS}$, $A16_{CAS}$			

- **Table 3-3** Nine-bit DRAM SIMM pinout (for implementing parity)

Pin #	SIMM Function	Processor Bus Function	Pin #	SIMM Function	Processor Bus Function
1	+5V	+5V	17	RA8	$A19_{RAS}$, $A18_{CAS}$
2	CAS~	CASLL~, CASLM~, CASUM~ *or* CASUU~	18	RA9	$A21_{RAS}$, $A20_{CAS}$
			19	RA10	$A23_{RAS}$, $A22_{CAS}$
3	DQ0	D0, D8, D16, *or* D24	20	DQ5	D5, D13, D21, *or* D29
4	RA0	$A6_{RAS}$, $A2_{CAS}$	21	WE~	RAMRW~
5	RA1	$A7_{RAS}$, $A3_{CAS}$	22	+5V	+5V
6	DQ1	D1, D9, D17, *or* D25	23	DQ6	D6, D14, D22, *or* D30
7	RA2	$A8_{RAS}$, $A4_{CAS}$	24	RA11	$A24_{RAS}$, $A25_{CAS}$
8	RA3	$A9_{RAS}$, $A5_{CAS}$	25	DQ7	D7, D15, D23, *or* D31
9	GND	GND	26	PDO	PDO0, PDO1, PDO2,
10	DQ2	D2, D10, D18, or D26			*or* PDO3
11	RA4	$A11_{RAS}$, $A10_{CAS}$	27	RAS~	RAS0~, *or* RAS1~
12	RA5	$A13_{RAS}$, $A12_{CAS}$	28	PCAS~	CASLL~, CASLM~,
13	DQ3	D3, D11, D19, or D27			CASUM~ *or* CASUU~
14	RA6	$A15_{RAS}$, $A14_{CAS}$	29	PD	PD0, PD1, PD2, *or*
15	RA7	$A17_{RAS}$, $A16_{CAS}$			PD3
16	DQ4	D4, D12, D20, *or* D28	30	+5V	+5V

Parity and the PGC

Parity is generated by the optional Parity Generator Chip (PGC). If you want parity checking you must order the Macintosh IIci configured with the PGC and nine-bit DRAM SIMMs.

On all reads in the RAM address space, the PGC generates an internal parity bit from each byte of the data bus, and compares it to the bit read from SIMM's parity bit. If the two parity bits do not agree, and parity is enabled, the PGC generates a parity error.

Note that parity is *always* written to the parity bit if the PGC is present. If the bit is not physically present on the SIMM module, it is simply ignored—a problem only exists if parity is *read* from the bit (i.e., parity is enabled) when the bit is not present (i.e., eight-bit DRAM SIMMs are in use).

Parity checking starts out disabled; the startup code will determine if the PGC is installed, and if parity memory is installed, and enable parity if appropriate. If a parity error is detected you will be told “A Memory Parity Error Has Occurred” and must reboot your Macintosh IIci.

Chapter 4 **The Cache Connector**

A cache card is a way of increasing system performance in the Macintosh IIci. The cache connector provides developers with infinite flexibility in implementing custom-designed cache hardware. The electrical and physical specifications of the cache connector and other implementation design considerations are provided in this chapter.

Designing For the Cache Connector

The Macintosh IIci is designed with a special purpose cache connector. The signals provided are optimized for a cache design, not a general purpose interface. A 120-pin EuroDIN connector is provided on the motherboard. This is the same connector as the SE/30 provides, but SE/30 cards are not compatible with the Macintosh IIci (see warning below). In addition to a new pinout, optimized for cache design, the Macintosh IIci cache connector is incompatible with the SE/30 due to:

- Different form factor: The space inside the Macintosh IIci differs from the SE/30.
- No space for an external connector: The Macintosh IIci has no back panel cutout for I/O connection to a card in the cache connector.
- Different clock speed: The Macintosh IIci runs at 25 MHz, rather than 16 MHz like the SE/30.
- Different Power Limit: 5 watts of power is allocated at +5 volts only.

♦ **Warning** The Macintosh IIci cache connector is not designed for SE/30 cards. The pinouts are different, so cards designed for the SE/30 will not work on Macintosh IIci, and may damage both the computer and the card. ♦

Do not cache accesses made by bus masters other than the 68030, since they may not know how to retry. Apple strongly suggests the use of synchronous logic (clocked by CPUCLK) on a cache card.

See Appendix A for detailed RAM and ROM waveforms. For information about using the Cache Connector for diagnostics, see Appendix B.

Use of a Cache

A cache card should operate transparently to user programs. The cache will be physical, as it has no access to the 68030's on-board MMU, so cache coherency should not be a problem. In addition, for a physical cache there should be no reason to flush the cache except when enabling the cache. The cache should also flush on a RESET~, but the system doesn't rely on this. The MMU table will mark the NuBus slot space and all I/O space as non-cacheable. Accesses to these locations by the 68030 will not be cached.

Accessing the Card

Address space has been reserved for use by the cache card, allowing test software to access both cache data memory and cache tag memory. Cache data should be accessed in the range from $5200 0000 through $527F FFFF (8 MB maximum), and Tag memory should be accessed in the range from $5280 0000 through $52FF FFFF (8 MB maximum). Cache cards must decode these address ranges themselves; no select signal is provided on the connector. Note that the cache card's address space is not accessible through the 24-bit memory map. Test software running in 24-bit mode must use the `SwapMMUMode` trap to enter 32-bit mode before it can access cache card memory.

- **Table 4-1** Cache address space

	From	To
Cache Data Memory	$5200 0000	$527F FFFF
Cache Tag Memory	$5280 0000	$52FF FFFF

Cache card enable, disable, and flush are controlled by ROM traps. They are called using a selector off the `HWPriv` (A098) trap.

- **Table 4-2** Cache control trap

Function	Selector
EnableExtCache	4
DisableExtCache	5
FlushExtCache	6

The organization of a particular card's data and tag memory will be determined by the card. System software will not make any assumptions about the cache card's organization, and only the card's test software should directly access cache card RAM.

Electrical Design Guidelines

The Macintosh IIci cache connector has a pinout specifically tailored to a cache implementation. The only unusual signal on the cache connector is CACHE. This active high signal disables the memory controller (MDU), so that it will not start a memory cycle and will allow the cache to supply the data instead. The active high CACHE signal must transition at the same time as the active low address strobe (AS~), or earlier. Asserting CACHE prevents the memory controller from beginning a RAM, ROM, or NuBus cycle. If CACHE is asserted after the memory controller has started a cycle, that cycle is not affected. CACHE has no effect on memory controller cycles for I/O devices. Since CACHE must be asserted at AS~, a cache controller will most likely leave CACHE asserted except when the cache is not active (e.g., CIOUT~ is asserted, CENABLE~ is negated, or an alternate bus master owns the bus as indicated by an asserted BGACK~ signal).

Note that NuBus cards can access each other without that transaction appearing on the CPU bus. This can lead to inconsistencies between memory on a NuBus card, for example, and the cached version of that memory. For this reason, the operating system always marks the NuBus address space as non-cacheable, as controlled by the MC68030's on-chip memory management unit (MMU).

The BGACK~ signal is not driven high quickly enough by the motherboard. The cache card should pull BGACK~ up to +5 V with a 2.2 K-ohm resistor, and double-rank synchronize BGACK~ before using it. To double-rank synchronize, put BGACK~ through two DQ flip-flops clocked by CPUCLK, and use the output from the second flip-flop.

Table 4-3 gives details of each cache connector signal. The category labeled "I/O" indicates Input or Output (or both, in some cases) from the cache card's point of view. "Motherboard Drives" specifies the current that the motherboard is able to supply, and the capacitive loading that the motherboard can tolerate. "Card Drives" specifies the current that the card must be able to supply, and the maximum capacitive loading that the motherboard would exhibit. "Master Drives" is applicable to input signals and "Card Drives" is applicable to output signals; thus, signals which are only input or output will have the appropriate driving specification left blank.

Most of the cache connector signals are designed to drive two 74LS inputs (a standard 74LS input load is 20 µA high, 0.2 mA low). Some exceptions will drive only one 74LS input,. These are: RESET~; the high order data byte (D24-D31); and the function codes (FC0-FC2). CPUCLK will drive only a CMOS input (a standard CMOS input load is 10 µA high, 10 µA low).

Refer to Appendix C for the timing diagrams of the cache card connector signals.

- **Table 4-3** Cache connector signals

Signal Name	Signal Description	I/O	Motherboard Drives	Card Drives	Motherboard Note	Pins
A0-A31	Address Bus	I	40 µA/0.4 mA 30 pF		1 KΩ Pullup (A30-A31 only)	32

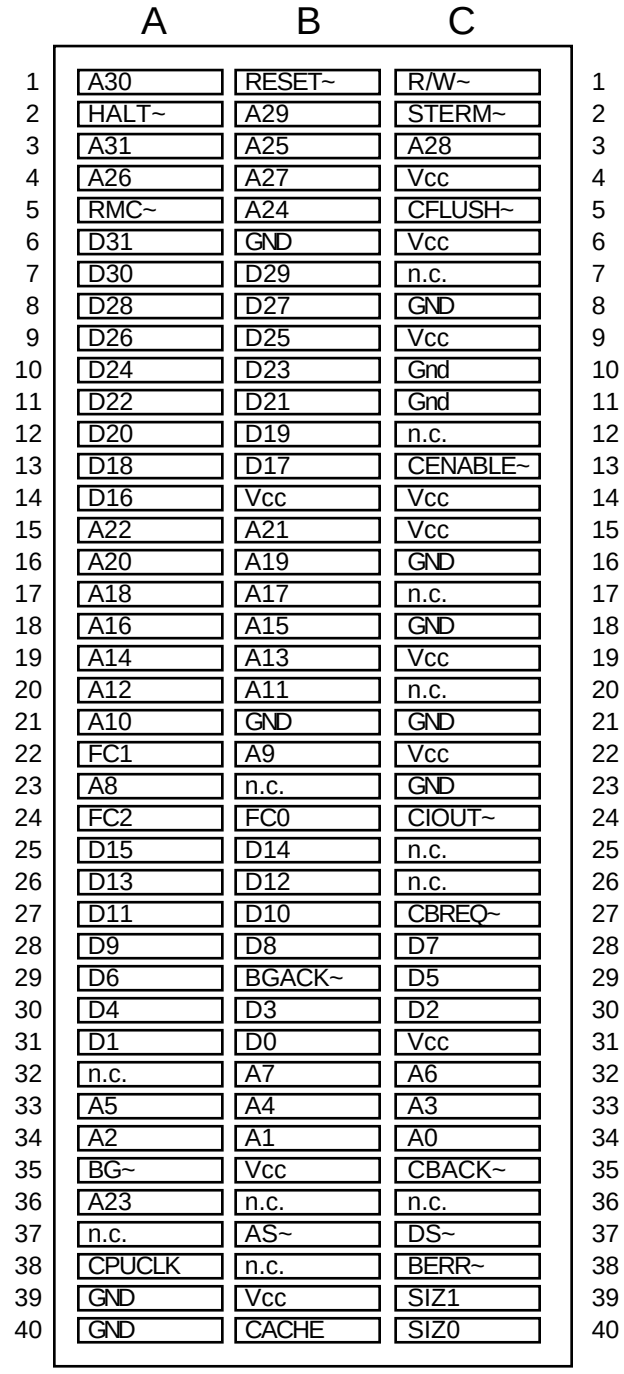
D0-D23 D24-D31	Data Bus	I/O	40 µA/0.4 mA 30 pF 20 µA/0.2 mA 15 pF	150 µA/1 mA 100 pF 300 µA/1 mA 100 pF		24 8
RESET~	Reset	I	20 µA/0.2 mA 15 pF		Open Collector 470Ω pullup	1
BERR~	Bus Error	I/O	40 µA/0.4 mA 30 pF	100 µA/8 mA 50 pF	1 KΩ pullup	1
HALT~	Halt	I/O	40 µA/0.4 mA 30 pF	100 µA/8 mA 50 pF	1 KΩ pullup	1
FC0-FC2	Function Codes	I	20 µA/0.2 mA 30 pF		1 KΩ pullup	3
BG~	Bus Grant	I	40 mA/0.4 mA 30 pF			1
BGACK~	Bus Grant Acknowledge	I	40 mA/0.4 mA 30 pF			1
SIZ0-SIZ1	Transfer Size	I	40 µA/0.4 mA 30 pF			2
AS~	Address Strobe	I	40 µA/0.4 mA 30 pF		1 KΩ pullup	1
R/W~	Read/Write	I	40 µA/0.4 mA 30 pF		1 KΩ pullup	1
STERM~	Synchronous Termination	I/O	40 µA/0.4 mA 30 pF	100 µA/8 mA 50 pF	1 KΩ pullup	1
CBACK~	Cache Burst Acknowledge	I	40 µA/0.4 mA 30 pF		1 KΩ pullup	1
CBREQ~	Cache Burst Request	I	40 µA/0.4 mA 30 pF		1 KΩ pullup	
CIOUT~	Cache Inhibit Out	I	40 µA/0.4 mA 30 pF		1 KΩ pullup	1
DS~	Data Strobe	I	40 µA/0.4 mA 30 pF		1 KΩ pullup	
RMC~	Read Modify write Cycle	I	40 µA/0.4 mA 30 pF		1 KΩ pullup	
CPUCLK	CPU Clock (25 MHz)	I	10µA/10µA 15 pF			1
CACHE	Memory Controller Disable for Cache Access	O		8 mA/1 mA 30 pF	1 KΩ pulldown	1
CFLUSH~	Cache Flush	I	40 µA/0.4 mA 30 pF			1

CENABLE~	Cache Enable	I	40 µA / 0.4 mA 30 pF			1
n.c.	no connection					15
Vcc	+5 volts	I	1 A			11
GND	Ground (Vss)	I				11

- **Table 4-4** Cache connector pinout

A		B		C
A30	1	RESET~	1	R/W~
HALT~	2	A29	2	STERM~
A31	3	A25	3	A28
A26	4	A27	4	Vcc
RMC~	5	A24	5	CFLUSH~
D31	6	GND	6	Vcc
D30	7	D29	7	n.c.
D28	8	D27	8	GND
D26	9	D25	9	Vcc
D24	10	D23	10	GND
D22	11	D21	11	GND
D20	12	D19	12	n.c.
D18	13	D17	13	CENABLE~
D16	14	Vcc	14	Vcc
A22	15	A21	15	Vcc
A20	16	A19	16	GND
A18	17	A17	17	n.c.
A16	18	A15	18	GND
A14	19	A13	19	Vcc
A12	20	A11	20	n.c.
A10	21	GND	21	GND
FC1	22	A9	22	Vcc
A8	23	n.c.	23	GND
FC2	24	FC0	24	CIOUT~
D15	25	D14	25	n.c.
D13	26	D12	26	n.c.
D11	27	D10	27	CBREQ~
D9	28	D8	28	D7
D6	29	BGACK~	29	D5
D4	30	D3	30	D2
D1	31	D0	31	Vcc
n.c.	32	A7	32	A6
A5	33	A4	33	A3
A2	34	A1	34	A0
BG~	35	Vcc	35	CBACK~
A23	36	n.c.	36	n.c.
n.c.	37	AS~	37	DS~
CPUCLK	38	n.c.	38	BERR~
GND	39	Vcc	39	SIZ1
GND	40	CACHE	40	SIZ0

- **Figure 4-1** Cache connector pin diagram



	A	B	C	
1	A30	RESET~	R/W~	1
2	HALT~	A29	STERM~	2
3	A31	A25	A28	3
4	A26	A27	Vcc	4
5	RMC~	A24	CFLUSH~	5
6	D31	GND	Vcc	6
7	D30	D29	n.c.	7
8	D28	D27	GND	8
9	D26	D25	Vcc	9
10	D24	D23	Gnd	10
11	D22	D21	Gnd	11
12	D20	D19	n.c.	12
13	D18	D17	CENABLE~	13
14	D16	Vcc	Vcc	14
15	A22	A21	Vcc	15
16	A20	A19	GND	16
17	A18	A17	n.c.	17
18	A16	A15	GND	18
19	A14	A13	Vcc	19
20	A12	A11	n.c.	20
21	A10	GND	GND	21
22	FC1	A9	Vcc	22
23	A8	n.c.	GND	23
24	FC2	FC0	CIOUT~	24
25	D15	D14	n.c.	25
26	D13	D12	n.c.	26
27	D11	D10	CBREQ~	27
28	D9	D8	D7	28
29	D6	BGACK~	D5	29
30	D4	D3	D2	30
31	D1	D0	Vcc	31
32	n.c.	A7	A6	32
33	A5	A4	A3	33
34	A2	A1	A0	34
35	BG~	Vcc	CBACK~	35
36	A23	n.c.	n.c.	36
37	n.c.	AS~	DS~	37
38	CPUCLK	n.c.	BERR~	38
39	GND	Vcc	SIZ1	39
40	GND	CACHE	SIZ0	40

Power Consumption Guidelines

The Macintosh IIci cache connector provides only +5 volts for cache card power. 5 watts of power are available for a cache card. Guidelines for power consumption are detailed in Table 4-5.

- **Table 4-5** Cache connector power consumption limits

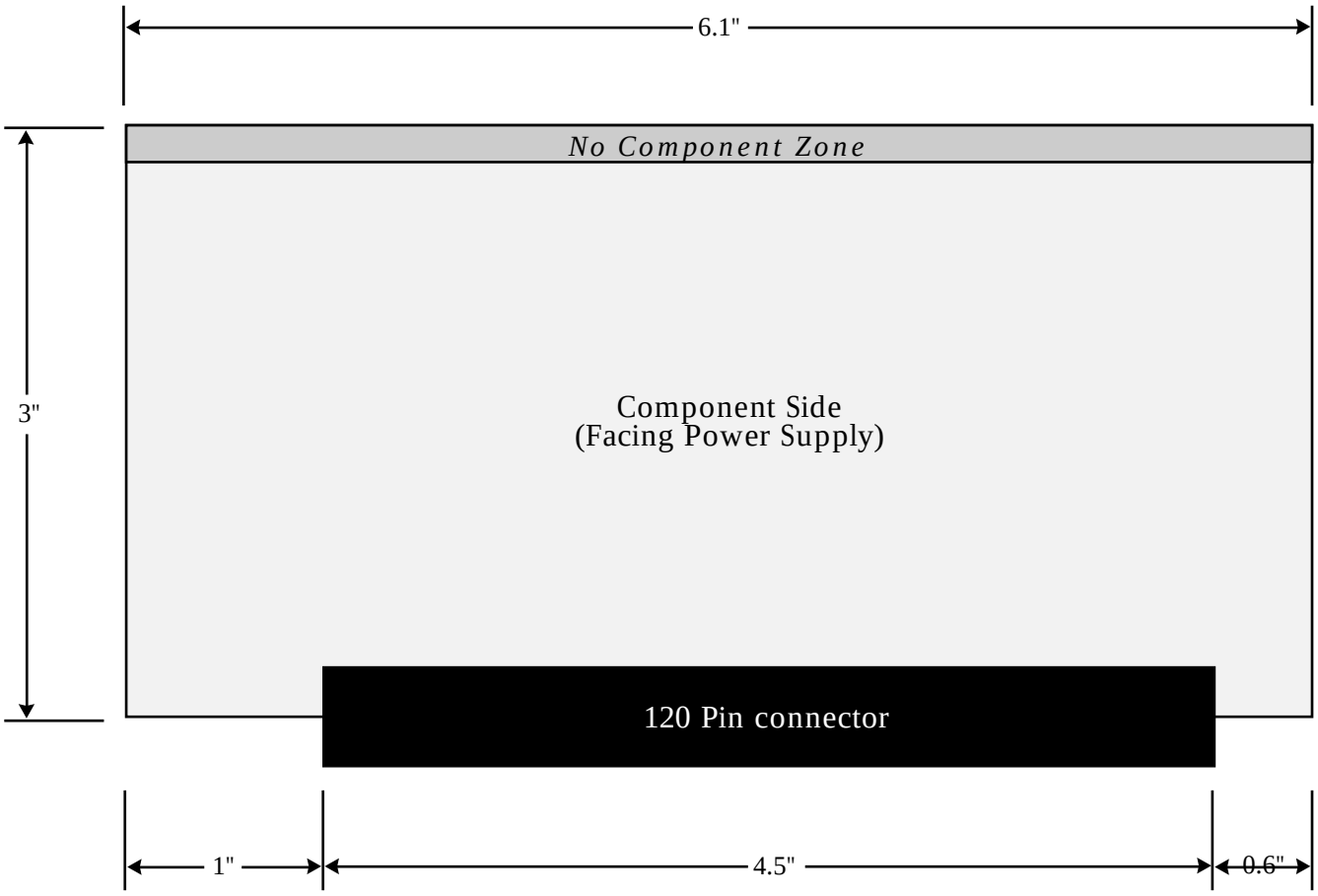
Device:	At +5 V	At +12 V	At -12 V
Each NuBus Card	2.0 A	0.175 A	0.150 A
Cache Card	1.0 A	*not available*	*not available*

♦ **Warning** Exceeding these guidelines will create potential reliability problems for your customer. ♦

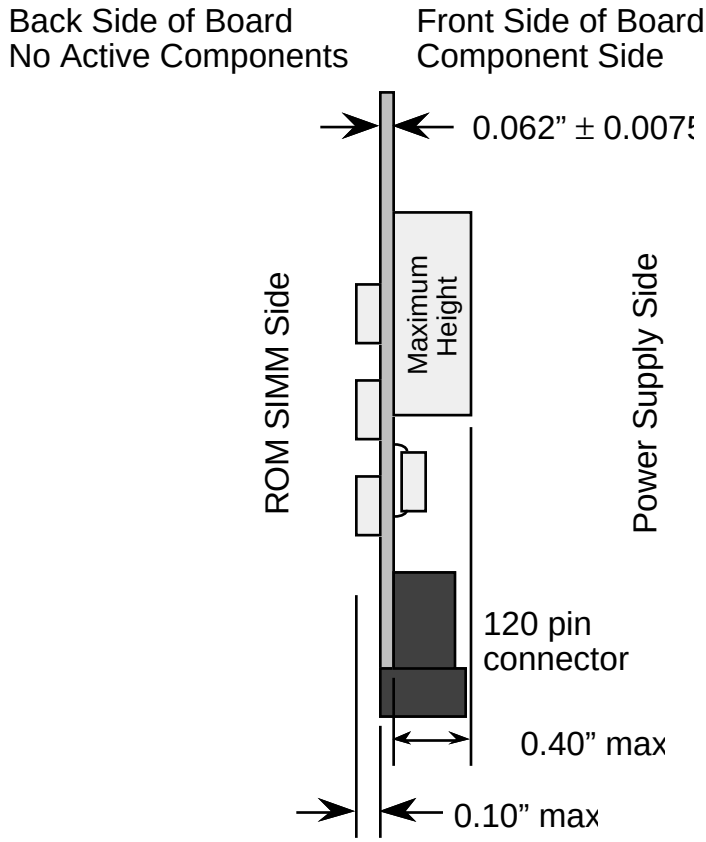
Mechanical Specifications

The maximum dimensions of the cache card are 3.0 inches in height and 6.1 inches in length, with the connector located as pictured below. These limitations are required for proper cooling. Cards not conforming to these guidelines will potentially create reliability problems for the customer. Note that the location of the connector is given with reference to the edge of the connector, *not* to pin A1.

- **Figure 4-2** Cache card dimensions, component-side view



- **Figure 4-3** Cache card dimensions, end view (from front of computer)



Card thickness must be 0.062±0.0075 inches. Warpage must be controlled to within 0.10 inch deviation from ideal.

The component placement specification for the cache card is not yet complete. Until such a specification is final, Apple suggests that you place no components or traces in the top 0.150 inch of the card, on either side. This is to allow Apple to provide additional stabilization for the card, if necessary.

Components may not extend beyond the edge of the card in any direction. Components height must not exceed 0.40 inch on the front side (toward the power supply), measured from the card surface. On the bottom side of the card (toward the ROM SIMM), no component or wire lead is allowed to extend more than 0.10 inch from that surface of the card.

No active components may be placed on the back side of the board; only resistors and capacitors which do not extend more than 0.10 inch above the surface of the board may be located on the back “non-component” side of the board.

Following these guidelines is important in order to allow proper thermal dissipation and in order not to interfere mechanically or electrically with the ROM SIMM.

EMI, Heat Dissipation, and Product Safety

See the guidelines in *Designing Cards and Drivers For the Macintosh Family, second edition* for these topics. Note that the maximum power dissipation is 5 watts for the cache connector, rather than the 7.5 watts specified for the SE/30 PDS connector.

Chapter 5 **The Video Interface**

Unlike previous Macintosh II models, the Macintosh IIci incorporates video on the main logic board. The on-board video supports many of the Apple Macintosh video monitors. The video electrical and physical specifications are provided in this chapter.

On-board Video

In addition to the existing NuBus video options, a new video solution has been built in to the Macintosh IIci, supporting the Macintosh II 12" B&W or 13" RGB and the 15" B&W Portrait monitors. The video signals are generated by the Apple custom RAM-Based Video (RBV) chip, and are driven through a CLUT/VDAC chip. Each monitor identifies itself by grounding certain pins on the RBV which then automatically selects the appropriate pixel clock and sync timing parameters. See "Video Cables" later in this chapter for cable wiring details.

When no monitor is plugged in, on-board video is halted. As shown in Table 5-1, the MON.ID bits can specify 8 possible combinations, each of may indicate a particular monitor.

- **Table 5-1** MON.ID values

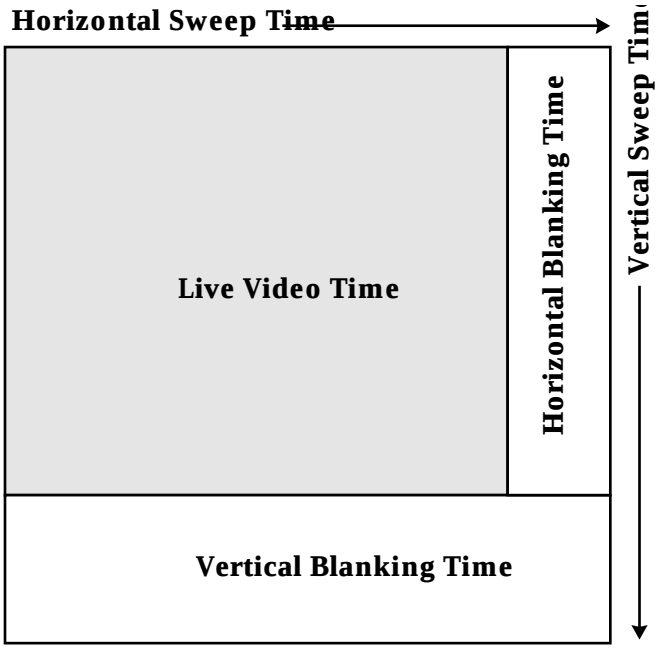
MON ID3	MON ID2	MON ID1	Monitor Selected
0	0	0	Unsupported monitor (video halted)
0	0	1	15" B&W Portrait Monitor
0	1	0	RESERVED for use by Apple
0	1	1	Unsupported monitor (video halted)
1	0	0	Unsupported monitor (video halted)
1	0	1	RESERVED for use by Apple
1	1	0	Macintosh II 12" B&W, 13" RGB
1	1	1	No external monitor (video halted)

The RBV and Bank A of DRAM share a separate RAM data bus, which can be connected to or disconnected from the CPU data bus by F245 bus buffers (see “Use of RAM by Video” in Chapter 3, “The RAM Interface”.) Data stored in Bank A of system DRAM is used by the RBV to feed a constant stream of video data to the display monitor during the live video portion of each horizontal screen line. The RBV asks the MDU for data as it is needed; the MDU responds by disconnecting the RAM data bus from the CPU data bus and performing an eight-long-word DMA burst read from RAM while clocking the read data into the RBV FIFO.

If a video burst is in progress, a CPU access to RAM Bank A is delayed, effectively slowing down the CPU. This effect is more pronounced for the larger monitors and for more bits per pixel as you can see in Figure 5-1. Note that only accesses to RAM Bank A are affected by video. The optional Bank B of DRAM connects directly to the CPU data bus, and the CPU has full access to this bank at all times, as it does to ROM and the I/O devices.

Figure 5-1 shows the time spent displaying video (labeled “Live Video Time”), and the time spent during blanking when no video memory accesses are occurring (labeled “Horizontal Blanking Time” and “Vertical Blanking Time”).

- **Figure 5-1** Video timing (not to scale)

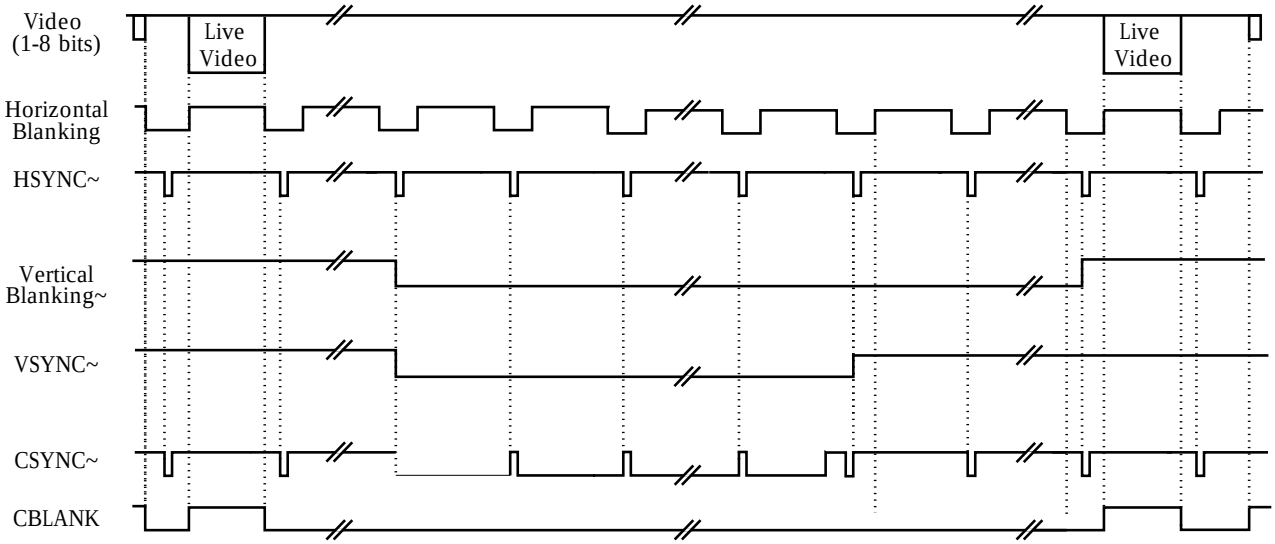


The RBV knows nothing about screen mapping or video addresses. Likewise, the MDU knows nothing about video. Each simply follows a protocol for passing data. The RBV drives certain signals based on the monitor indicated by the Monitor ID bits (see Table 5-2). The video signals are pictured in detail on the following pages. The Monitor ID (MON.ID1-3) is asserted by the monitor by grounding lines for 0's and leaving no connects for 1's.

- **Table 5-2** RBV signal descriptions

MON ID 321	Monitor Selected	Signals Driven	Signals Stopped	Cols/ Rows	Dot Clock/ Dot	Line/ Rate	Frame/ Rate
0 0 1	15" Portrait	VID.OUT(0-7)	CSYNC~ = 1	640	57.2832 MHz	14.52 µs	13.33 ms
		CBLANK~		870	17.457 ns	68.850 KHz	75 Hz
		HSYNC~					
		VSYNC~					
0 1 0	RESERVED						
1 0 1							
1 1 0	12" B/W,	VID.OUT(0-7)	HSYNC~ = 1	640	30.2400 MHz	28.57 µs	15.00 ms
	13" RGB	CBLANK~	VSYNC~ = 1	480	33.07 ns	35.0 KHz	66.67 Hz
		CSYNC~					
0 0 0	Video halted	None	VID.OUT(0-7) = 1's				
1 0 0			CBLANK~ = 0				
0 1 1			CSYNC~ = 1				
1 1 1			HSYNC~ = 1				
			VSYNC~ = 1				

- **Figure 5-2** Video signal sync timing



NOTES:

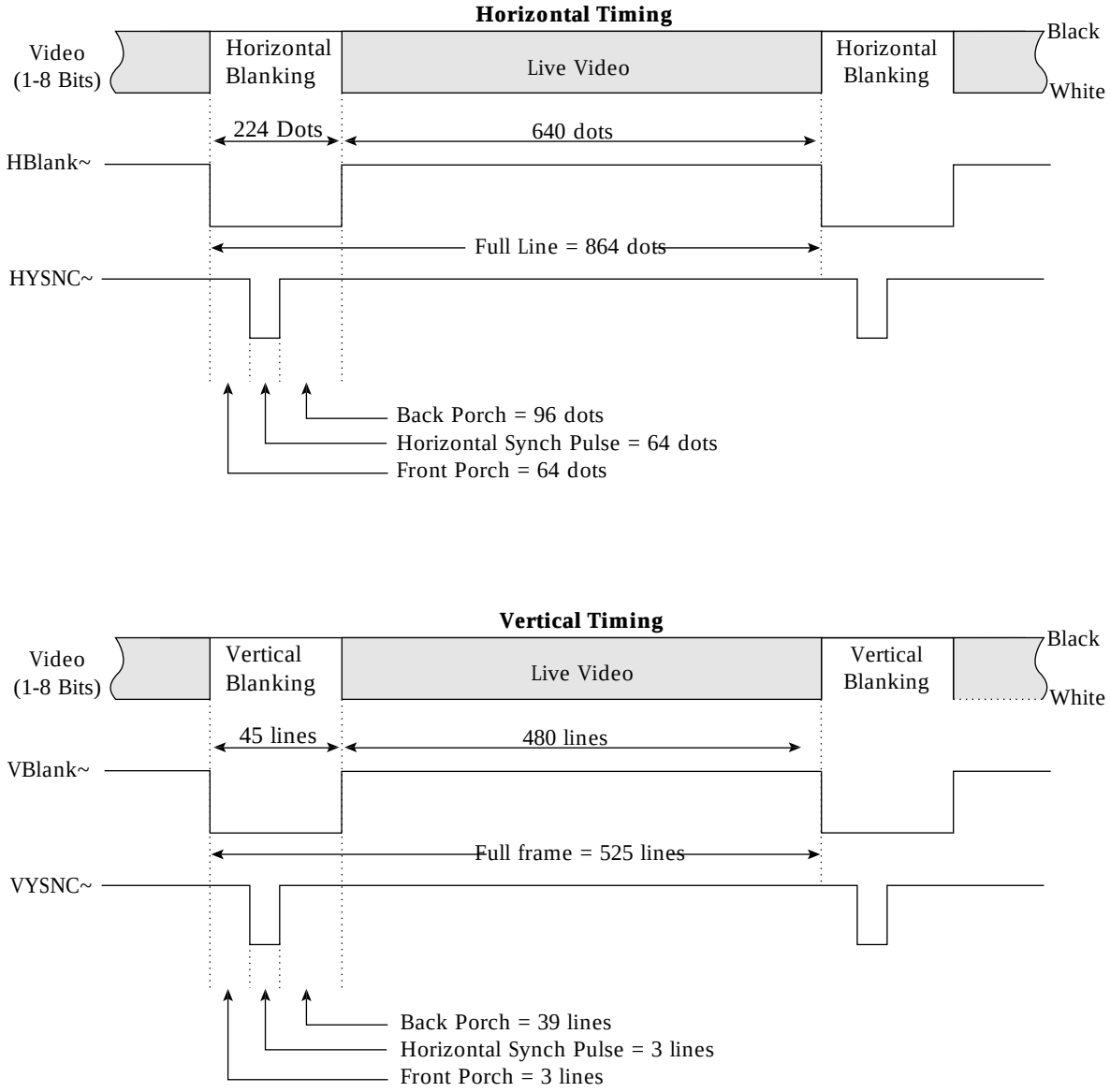
1. All signals change on the rising edge of the dot clock.

2. Signals with names in mixed case are used inside the RBV, and are not available on output pins.

3. The width of the pulse on CSYNC~ during VSYNC~ low is the same width as the HSYNC~ pulse (and therefore the width of the pulse on CSYNC~ during VSYNC~ high).

4. For the 12" RGB, 13" B&W, and 15" B&W Portrait monitors, both edges of VSYNC~ coincide with HSYNC~ falling.

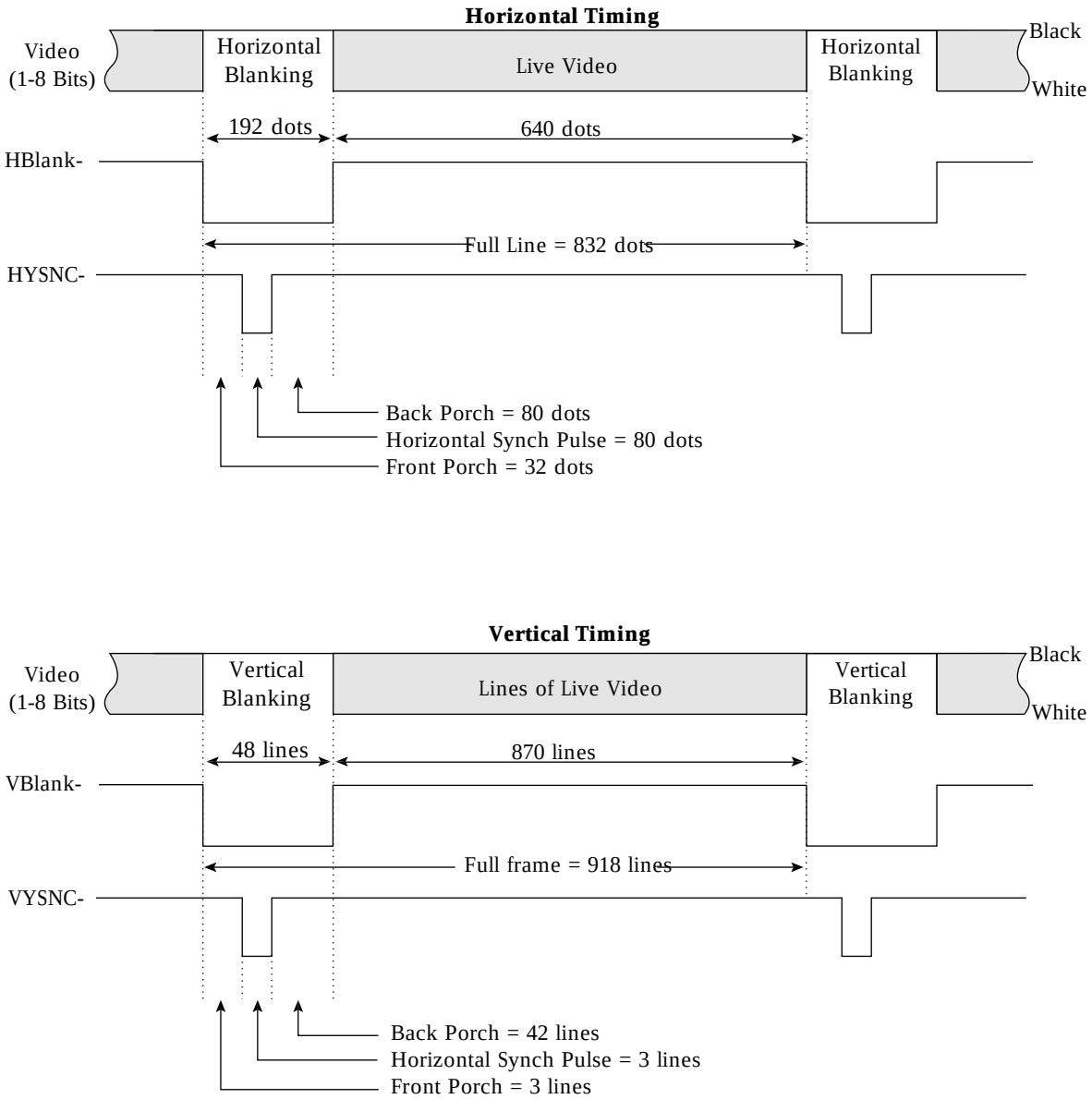
- **Figure 5-3** Video signal timing for the Apple 13-inch and 12-inch monitors.



Dot Clock = 30.2400 MHz±.196	Full Line = 28.57µS	Full Frame = 15.00 mS
Dot = 33.07 nS	Line Rate = 35.0 KHz	Frame Rate = 66.67 Hz

All timings are derived from the dot clock and have the same tolerance

- **Figure 5-4** Horizontal and vertical video signal timing for the Apple 15-inch Portrait Monitor.



Dot Clock= 57.2832 MHz±.196
Dot = 17.457ns

Full Line = 14.52µS
Line Rate = 68.850 KHz

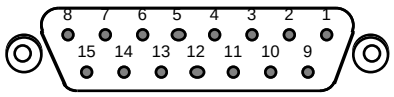
Full Rate = 13.33 mS
Frame Rate = 75 Hz

All timings are derived from the dot clock and have the same tolerance

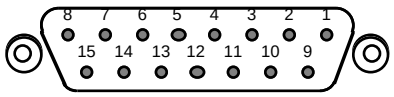
Video Cables

The video connector on the back of the Macintosh IIci is a DB-15, as shown in Figure 5-5. The connector on the monitor will be either a DB-15 (for the 12″ B&W and 13″ RGB monitors) as shown in Figure 5-6, or a D-25 (for the 15″ Portrait monitor), as in Figure 5-7. The DB-15 Monitor connector pin numbers are the same as the Macintosh IIci pin numbers, pin for pin.

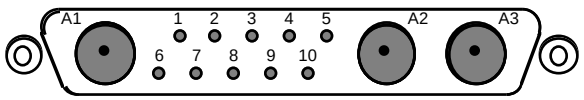
- **Figure 5-5** DB-15 Macintosh IIci Video Connector



- **Figure 5-6** DB-15 Monitor Video Connector



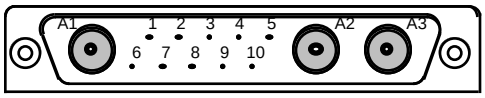
- **Figure 5-7** D-25 Monitor Video Connector

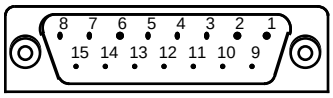


- **Table 5-3** Video connector and cable pinouts

Macintosh IIci DB-15 Pinout			12″ B&W, 13″ RGB	15″ B&W Portrait
Pin	Signal	Description		
1	RED.GND	Red Video Ground	RED.GND	n. c.
2	RED.VID	Red Video	RED.VID	n. c.
3	CSYNC~	Composite Sync	CSYNC~	n. c.
4	MON.ID1	Monitor ID, Bit 1	ID1.GND	n. c.
5	GRN.VID	Green Video	GRN.VID	n. c.
6	GRN.GND	Green Video Ground	GRN.GND	n. c.
7	MON.ID2	Monitor ID, Bit 2	n. c.	ID2.GND
8	n. c.	(no connection)	n. c.	n. c.
9	BLU.VID	Blue Video	BLU.VID	BLU.VID
10	MON.ID3	Monitor ID, Bit 3	n. c.	ID3.GND
11	C&VSYNC.GND	CSYNC & VSYNC Ground	CSYNC.GND	VSYNC.GND
12	VSYNC~	Vertical Sync	n. c.	VSYNC~
13	BLU.GND	Blue Video Ground	BLU.GND	BLU.GND
14	HSYNC.GND	HSYNC Ground	n. c.	HSYNC.GND
15	HSYNC~	Horizontal Sync	n. c.	HSYNC~
Shell	CHASSIS.GND	Chassis Ground	CHASSIS.GND	CHASSIS.GND

- **Table 5-4** Apple 15-inch Apple Portrait Monitor cable connections





Macintosh IIci D-25 Pin No.	Signal Name	Apple Portrait Monitor DB-15 Pin No.	
1	HSYNC.GND	14	
2	VSYNC~	12	
3	MON.ID3	10	
4	(no wire)	8	
5	CSYNC~	3	(note 1)
6	HSYNC~	15	
7	VSYNC.GND	11	(note 2)
8	MON.ID2	7	
9	MON.ID1		
10	CSYNC.GND	11	(notes 1 & 2)
A1 (center)	BLU.VID9		
A1 (outer)	BLU.GND13		
A2 (center)	GRN.VID5		(note 3)
A2 (outer)	GRN.GND6		(note 3)
A3 (center)	RED.VID2		(note 3)
A3 (outer)	RED.GND1		(note 3)
Shell	CHASSIS.GND	Shell	

NOTES:

1. The lines labelled CSYNC~ and CSYNC.GND are not needed for the 15″ Portrait or larger monitors because those monitors use separate VSYNC~ and HSYNC~ signals. CSYNC~ and CSYNC.GND are needed in the cable only for connecting a NuBus portrait video card's D-25 connector to a DB-15 connector.

2. Notice that CSYNC.GND and VSYNC.GND share the same pin on the DB-15 connector.

3. The green video and the red video coax cables are not needed for the black & white 15″ portrait monitor.

Chapter 6 **The NuBus Interface**

The NuBus expansion interface bus in the Macintosh IIci is the same design as used in the Macintosh IIcx, with few changes. The similarities and differences are detailed in this chapter.

NuBus Interface

The NuBus Interface as used in the Macintosh IIci remains the same as the Macintosh IIcx, except that the slots are numbered 4 through 6 and mapped to geographic addresses $C through $E. On the Macintosh IIcx, they were numbered 1 through 3 and mapped to geographic addresses $9 through $B. This should not matter to the cards. Additional information regarding the NuBus Interface can be found in the Apple publication *Designing Cards and Drivers For the Macintosh Family, second edition*. Power consumption guidelines are discussed in Chapter 4, "The Cache Connector."

- **Table 6-1** NuBus slot numbers

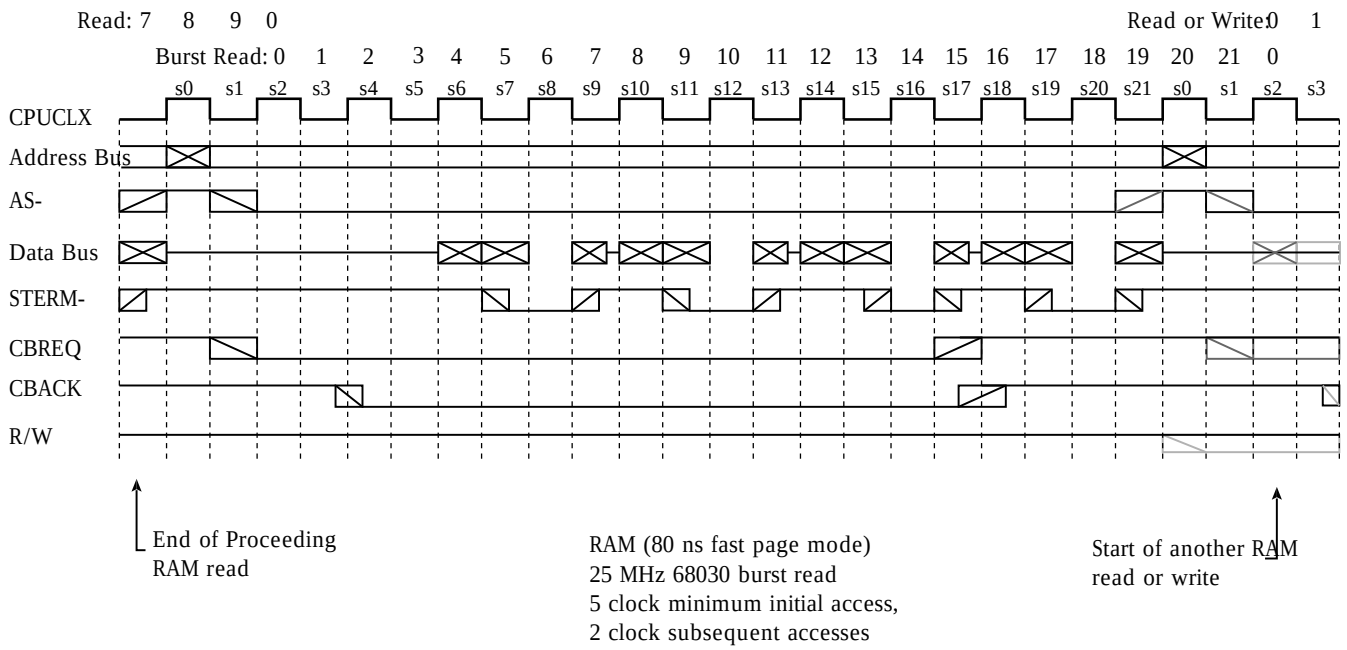
Slot Number	Geographic Address	Geographic Address Pins			
		GA3~	GA2~	GA1~	GA0~
4	$C	GND	GND	open	open
5	$D	GND	GND	open	GND
6	$E	GND	GND	GND	open

Appendix A **RAM and ROM Timing Diagrams**

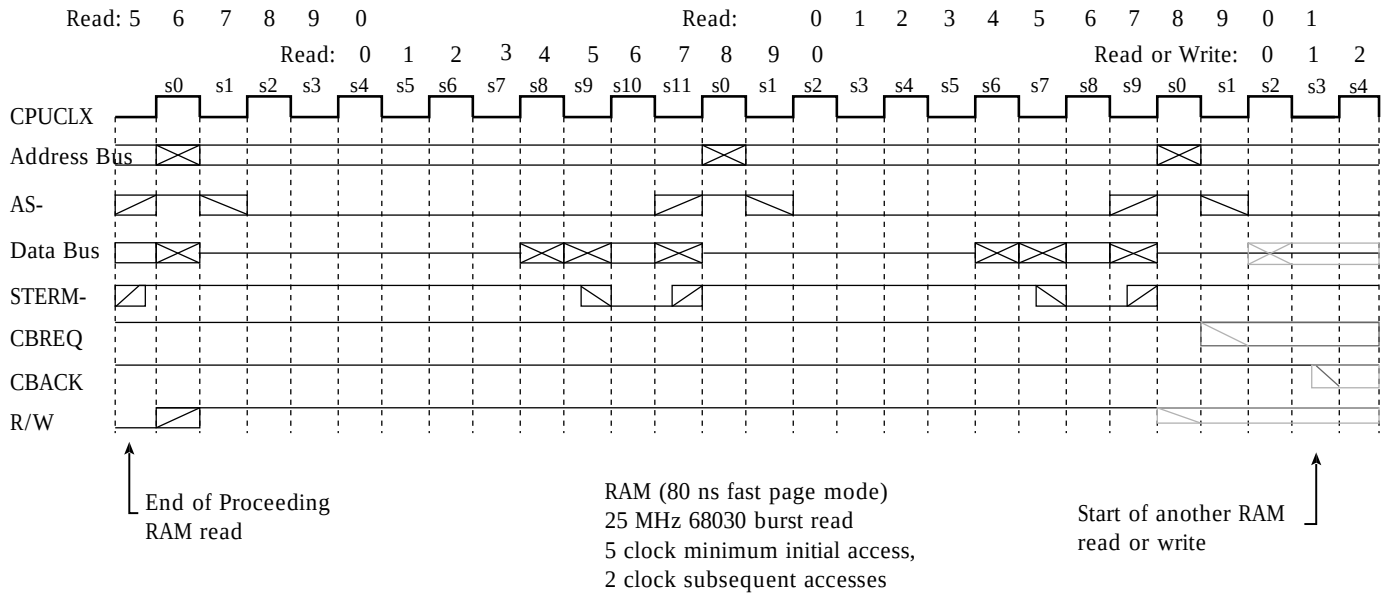
Timing diagrams for the RAM and ROM signals are provided in this appendix.

The following waveforms are idealized drawings of the RAM and ROM interfaces. The “s” numbers refer to the MC68030 states, while the large numbers refer to the MDU states. The timings are referenced to the CPUCLK. Both the rising and falling edges of the CPUCLK are used to change states.

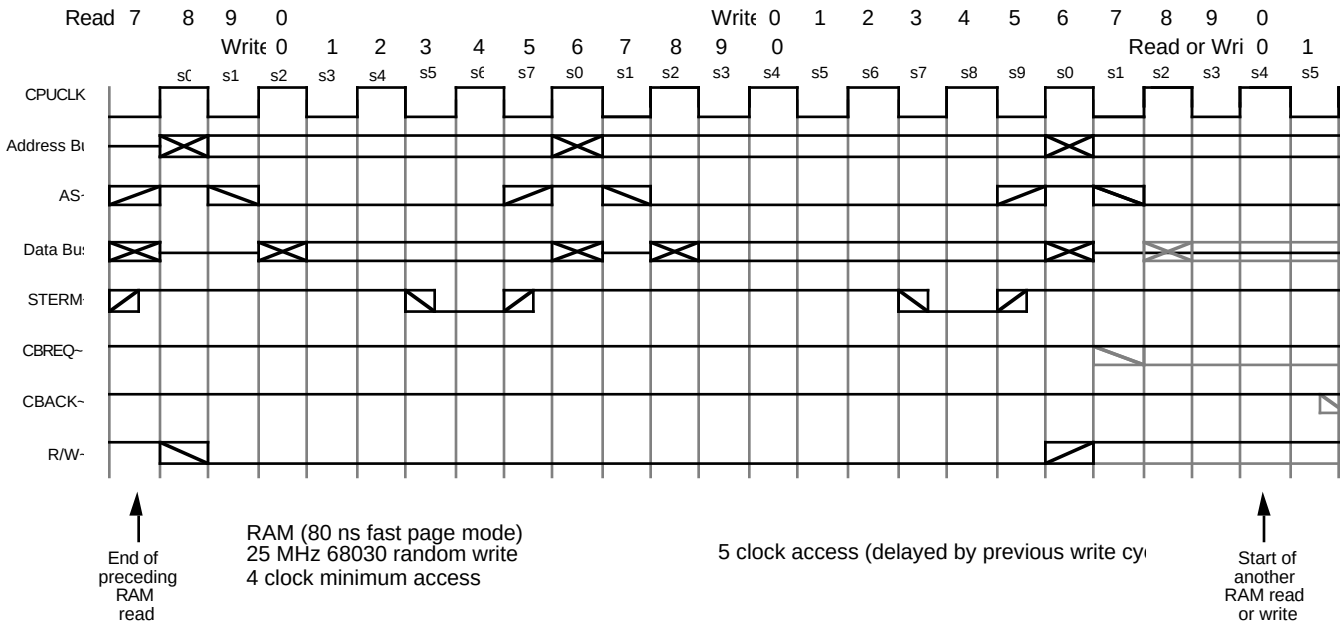
- **Figure A-1** RAM burst read timing



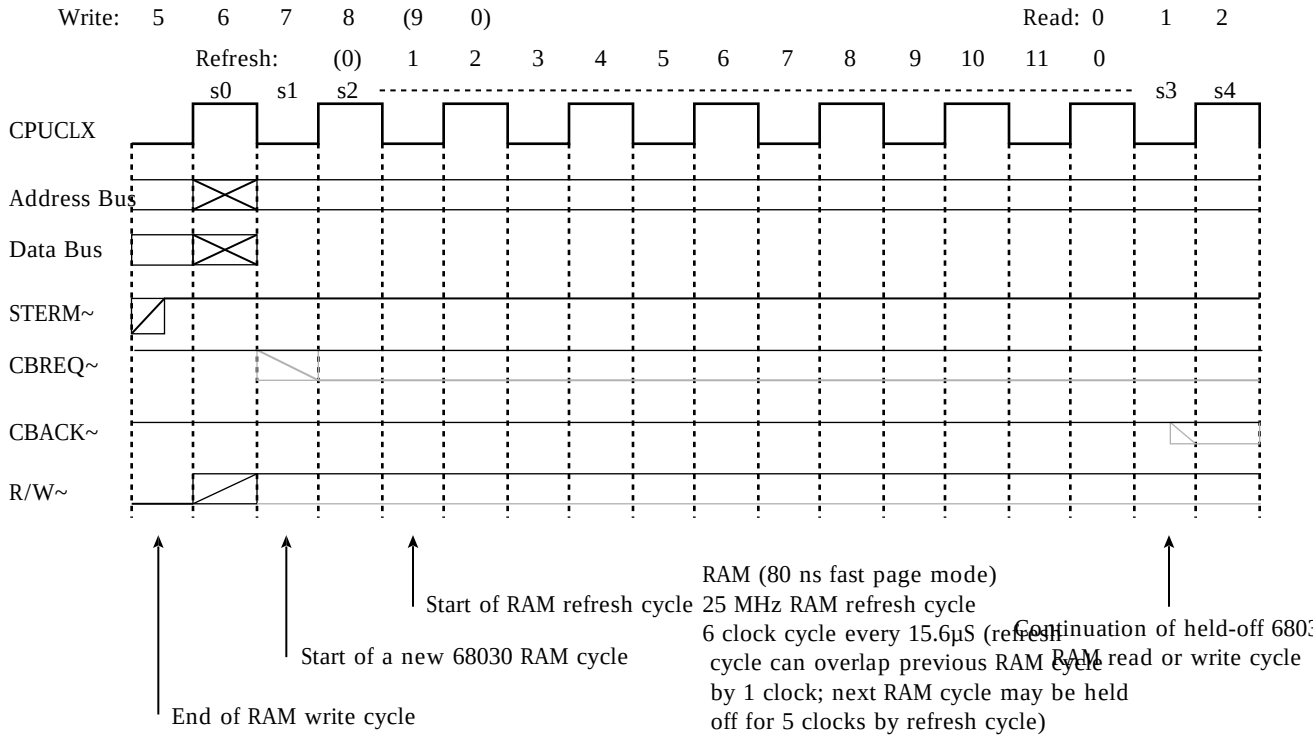
- **Figure A-2** RAM random read timing



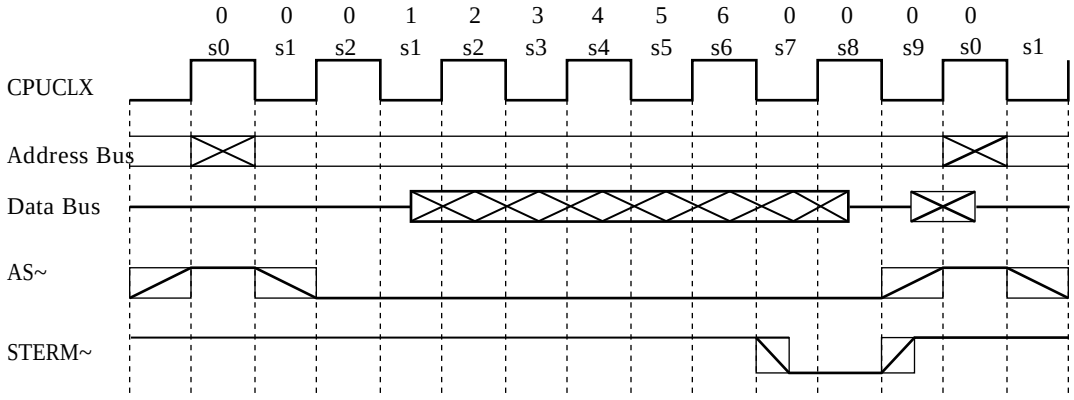
- **Figure A-3** RAM random write timing



- **Figure A-4** RAM refresh timing



- **Figure A-5** ROM read timing



Appendix B **Diagnostic Pinouts**

Additional signals are provided for Apple's internal use in debugging and for emulator support. These signals are documented in this chapter for developers to use to develop emulators and other hardware debugging tools.

The additional signals described in this appendix may not be supported in future implementations of the cache connector. They are provided only for debugging and emulator support. These are indicated in **bold** style and are referred to as "No Connection" on the cache connector pinout. Please note that while the connector is capable of other functionality, Apple intends to support its use for RAM cache products only. See Chapter 4, "The Cache Connector" for an explanation of these signals.

In the Table B-1, below, "I/O" refers to Input and Output from the cache card's point of view. "Motherboard Drives" specifies the current that the motherboard is able to supply, and the capacitive loading that the motherboard can tolerate. "Card Drives" specifies the current that the card must be able to supply, and the maximum capacitive loading that the motherboard would exhibit. "Master Drives" is applicable to input signals and "Card Drives" is applicable to output signals; thus, signals which are only input or output will have the appropriate driving specification left blank. Signals listed in parentheses are usually driven by the MC68030, but are rendered high-impedance by the MC68030 after granting the bus to a DMA requestor. When rendered high-impedance by the MC68030, these signals may be driven. The CPUDIS signal is used to disable the MC68030 on the mother board and render its outputs high-impedance. An emulator in the cache connector may assert CPUDIS and, after waiting for the end of the current bus cycle, may drive all signals.

- **Table B-1** Cache connector signal descriptions

Signal Name	Signal Description	I/O	Motherboard Drives	Card Drives	Motherboard Note	Pins
A0-A29	Address Bus	**I/(O)**	40 µA/0.4 mA 30 pF	**(300 µA/1 mA 100 pF)**		30
A30-A31		**I/(O)**	40 µA/0.4 mA 30 pF	**(300 µA/8 mA 100 pF)**	1KΩ Pullup	2
D0-D23	Data Bus	I/O	40 µA/0.4 mA 30 pF	150 µA/1 mA 100 pF		24
D24-D31			20 µA/0.2 mA 15 pF	300 µA/1 mA 100 pF		8

RESET~	Reset	**I/O**	20 µA/0.2 mA 15 pF	**N.A./15 mA** **50 pF**	Open Collector 470Ω pullup	1
BERR~	Bus Error	I/O	40 µA/0.4 mA 30 pF	100 µA/8 mA 50 pF	1 KΩ pullup	1
HALT~	Halt	I/O	40 µA/0.4 mA 30 pF	100 µA/8 mA 50 pF	1 KΩ pullup	1
FC0-FC2	Function Codes	**I/(O)**	20 µA/0.2 mA 15 pF	**(100 µA/8 mA** **50 pF)**	1 KΩ pullup	3
BR~	**Bus Request**	**I**	**40 µA/0.4 mA** **30 pF**		**1 KΩ** **pullup**	**1**
BG~	Bus Grant	**I/(O)**	40 µA/0.4 mA 30 pF	**(100 µA/8 mA** **50 pF)**	1 KΩ pullup	1
BGACK~	Bus Grant Acknowledge	I	40 µA/0.4 mA 30 pF			1
SIZ0-SIZ1	Transfer Size	**I/(O)**	40 µA/0.4 mA 30 pF	**(40 µA/0.4 mA** **30 pF)**		2
AS~	Address Strobe	**I/(O)**	40 µA/0.4 mA 30 pF	**(300 µA/8 mA** **100 pF)**	1 KΩ pullup	1
DSACK0~, **DSACK1~**	**Data Transfer and Size Acknowledge**	**I/O**	**40 µA/0.4 mA** **30 pF**	**100 µA/8 mA** **50 pF**	**1 KΩ** **pullup**	**2**
R/W~	Read/Write	**I/(O)**	40 µA/0.4 mA 30 pF	**(300 µA/8 mA** **100 pF)**	1 KΩ pullup	1
STERM~	Synchronous Termination	I/O	40 µA/0.4 mA 30 pF	100 µA/8 mA 50 pF	1 KΩ pullup	1
CBACK~	Cache Burst Acknowledge	**I/O**	40 µA/0.4 mA 30 pF	**100 µA/8 mA** **50 pF**	1 KΩ pullup	1
CBREQ~	Cache Burst Request	**I/(O)**	40 µA/0.4 mA 30 pF	**(100 µA/8 mA** **50 pF)**	1 KΩ pullup	1
CIOUT~	Cache Inhibit Out	**I/(O)**	40 µA/0.4 mA 30 pF	**(100 µA/8 mA** **50 pF)**	1 KΩ pullup	1
DS~	Data Strobe	**I/(O)**	40 µA/0.4 mA 30 pF	**(100 µA/8 mA** **50 pF)**	1 KΩ pullup	1
RMC~	Read Modify write Cycle	**I/(O)**	40 µA/0.4 mA 30 pF	**(100 µA/8 mA** **50 pF)**	1 KΩ pullup	1
IPL0~-IPL2~	**Interrupt Priority Lines**	**I**	**40 µA/0.4 mA** **30 pF**		**1 KΩ** **pullup**	**3**
CPUCLK	CPU Clock (25 MHz)	I	10µA/10µA 15 pF			1
ROMOE~	**ROM Output Enable**	**I**	**40 µA/0.4 mA** **30 pF**			**1**

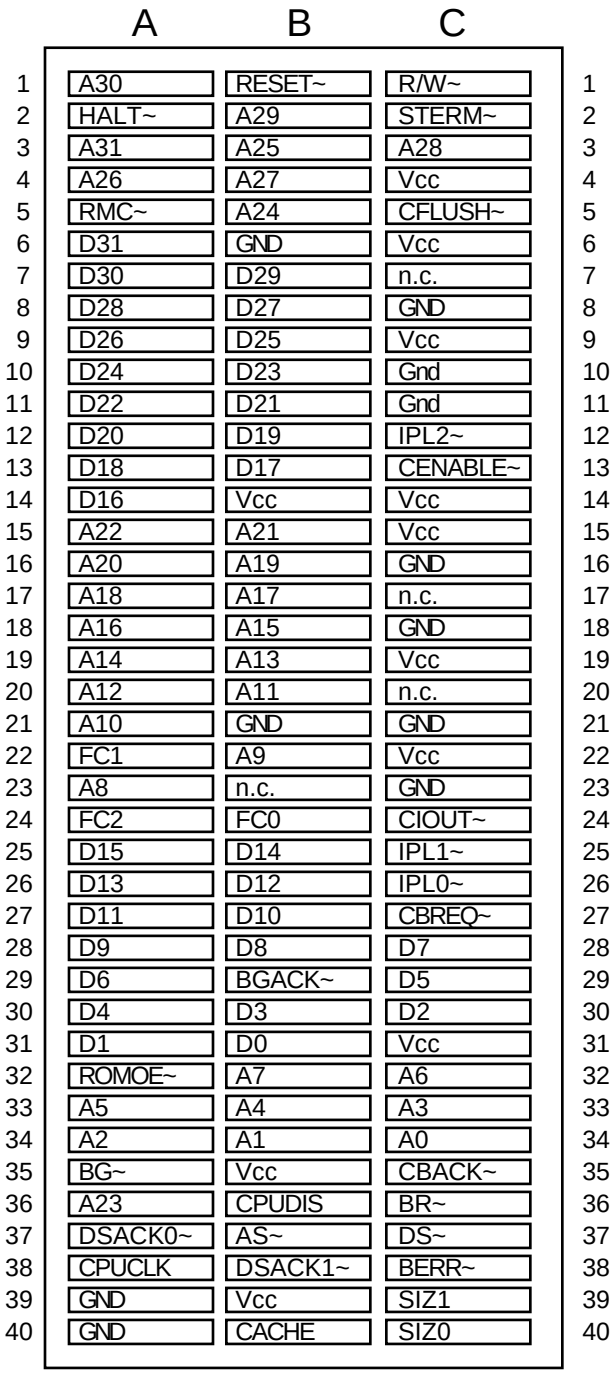
CPUDIS	**CPU Disable**	**O**		**8 mA/1 mA 30 pF**	**1 KΩ pulldown**	**1**
CACHE	Memory Controller Disable for Cache Access	O		8 mA/1 mA 30 pF	1 KΩ pulldown	1
CFLUSH~	Cache Flush	I	40 µA/0.4 mA 30 pF			1
CENABLE~	Cache Enable	I	40 µA/0.4 mA 30 pF			1
n.c.	no connection					4
Vcc	+5 volts	I	1 A			11
GND	Ground (Vss)	I				11

Pin names in **bold** style are only for debugging and emulator support. These are labeled "n.c." (no connection) on the cache connector pinout diagram.

- **Figure B-1** Cache connector pinout diagram

A		B		C
A30	1	RESET~	1	R/W~
HALT~	2	A29	2	STERM~
A31	3	A25	3	A28
A26	4	A27	4	Vcc
RMC~	5	A24	5	CFLUSH~
D31	6	GND	6	Vcc
D30	7	D29	7	n.c.
D28	8	D27	8	GND
D26	9	D25	9	Vcc
D24	10	D23	10	GND
D22	11	D21	11	GND
D20	12	D19	12	**IPL2~**
D18	13	D17	13	CENABLE~
D16	14	Vcc	14	Vcc
A22	15	A21	15	Vcc
A20	16	A19	16	GND
A18	17	A17	17	n.c.
A16	18	A15	18	GND
A14	19	A13	19	Vcc
A12	20	A11	20	n.c.
A10	21	GND	21	GND
FC1	22	A9	22	Vcc
A8	23	n.c.	23	GND
FC2	24	FC0	24	CIOUT~
D15	25	D14	25	**IPL1~**
D13	26	D12	26	**IPL0~**
D11	27	D10	27	CBREQ~
D9	28	D8	28	D7
D6	29	BGACK~	29	D5
D4	30	D3	30	D2
D1	31	D0	31	Vcc
ROMOE~	32	A7	32	A6
A5	33	A4	33	A3
A2	34	A1	34	A0
BG~	35	Vcc	35	CBACK~
A23	36	**CPUDIS**	36	**BR~**
DSACK0~	37	AS~	37	DS~
CPUCLK	38	**DSACK1~**	38	BERR~
GND	39	Vcc	39	SIZ1
GND	40	CACHE	40	SIZ0

- **Table B-2** Cache connector pin diagram



	A	B	C	
1	A30	RESET~	R/W~	1
2	HALT~	A29	STERM~	2
3	A31	A25	A28	3
4	A26	A27	Vcc	4
5	RMC~	A24	CFLUSH~	5
6	D31	GND	Vcc	6
7	D30	D29	n.c.	7
8	D28	D27	GND	8
9	D26	D25	Vcc	9
10	D24	D23	Gnd	10
11	D22	D21	Gnd	11
12	D20	D19	IPL2~	12
13	D18	D17	CENABLE~	13
14	D16	Vcc	Vcc	14
15	A22	A21	Vcc	15
16	A20	A19	GND	16
17	A18	A17	n.c.	17
18	A16	A15	GND	18
19	A14	A13	Vcc	19
20	A12	A11	n.c.	20
21	A10	GND	GND	21
22	FC1	A9	Vcc	22
23	A8	n.c.	GND	23
24	FC2	FC0	CIOUT~	24
25	D15	D14	IPL1~	25
26	D13	D12	IPL0~	26
27	D11	D10	CBREQ~	27
28	D9	D8	D7	28
29	D6	BGACK~	D5	29
30	D4	D3	D2	30
31	D1	D0	Vcc	31
32	ROMOE~	A7	A6	32
33	A5	A4	A3	33
34	A2	A1	A0	34
35	BG~	Vcc	CBACK~	35
36	A23	CPUDIS	BR~	36
37	DSACK0~	AS~	DS~	37
38	CPUCLK	DSACK1~	BERR~	38
39	GND	Vcc	SIZ1	39
40	GND	CACHE	SIZ0	40

Appendix C Cache signal timing diagrams

The cache card connector signal timing diagrams are provided in this appendix.

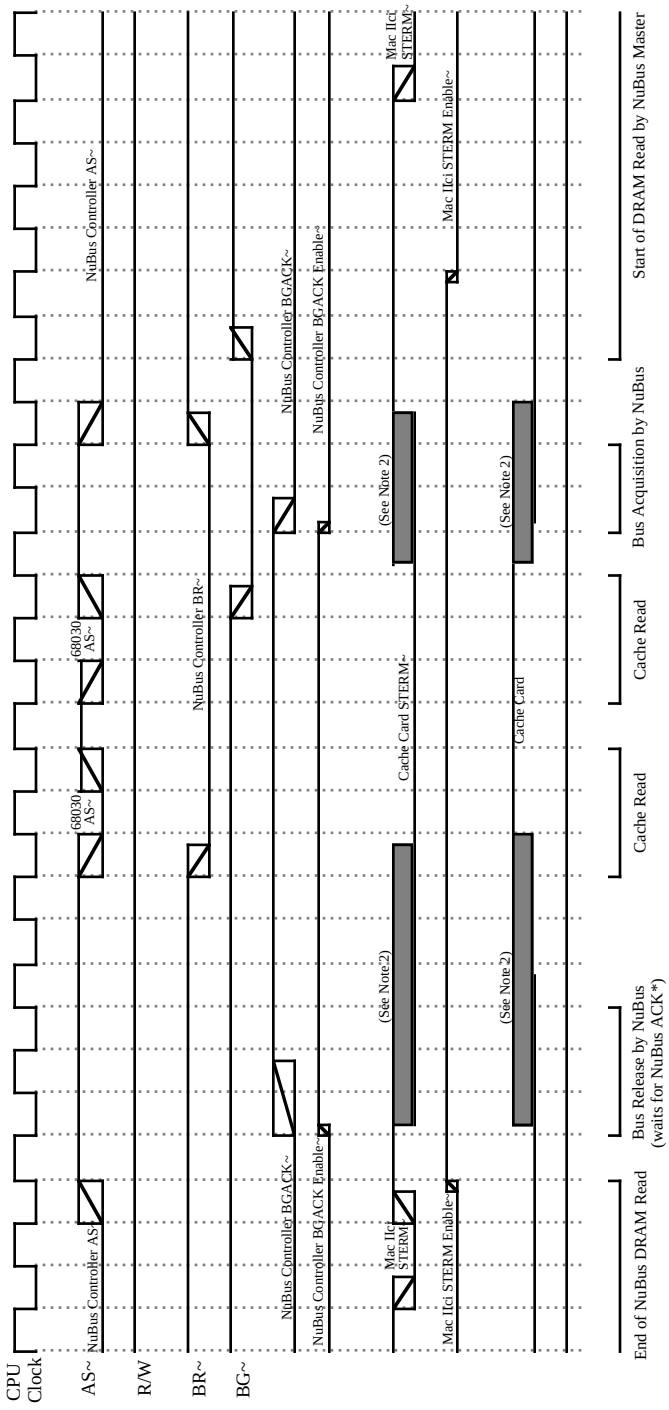
- **Figure C-1** Timing diagram showing the interaction between cache card signals and the optional Parity Generator Chip

Note 1: The cycles shown in this diagram are meant to show various possible relative timings of STERM~ and CACHE, as they affect parity checking in a Macintosh IIci with parity option. These cycles do not represent actual Macintosh IIci DRAM or cache card cycles.

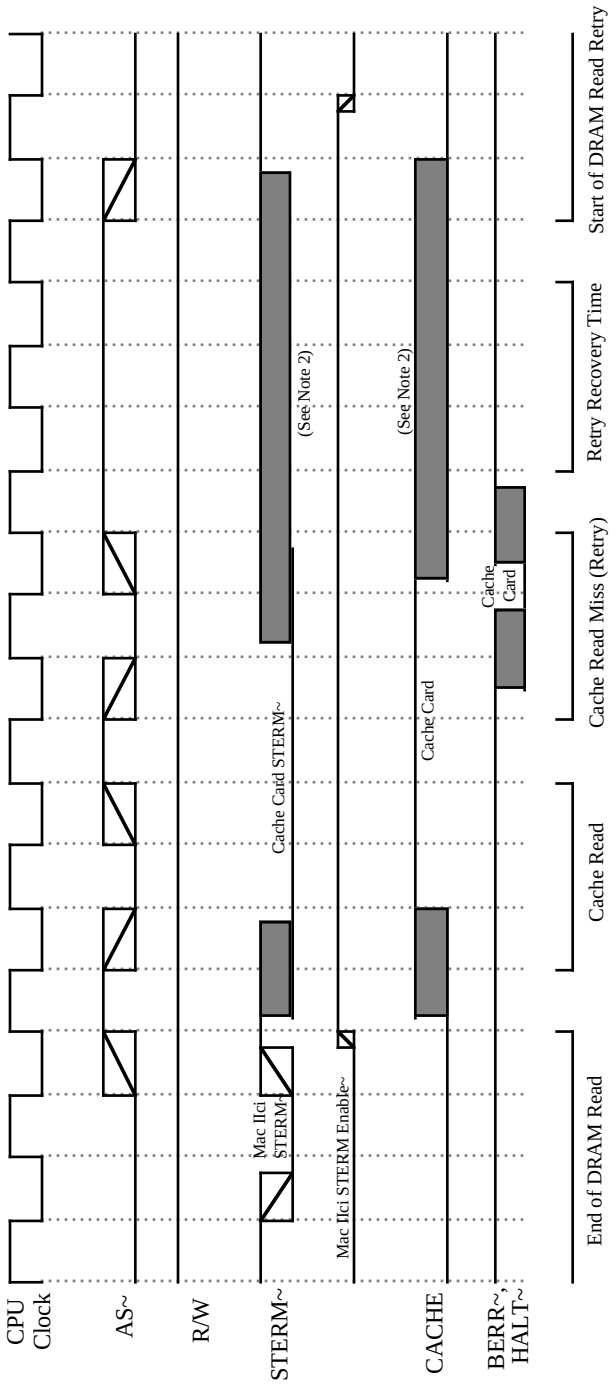
Note 2: In a Macintosh IIci with parity option, a parity error may occur if STERM~ is low at any rising edge of CPU clock unless:
1) valid DRAM data is present at the next falling edge, or
2) CACHE is high at the next falling edge, or
3) CACHE was high at the previous falling edge.

Note 3: Parity errors are not generated for writes, for accesses outside of the DRAM physical address space ($0000 0000 through $07FF FFFF), or when parity checking is disabled.

- **Figure C-2** Timing diagram showing the interaction between a generic cache card's signals and the Macintosh IIci's NuBus connector signals



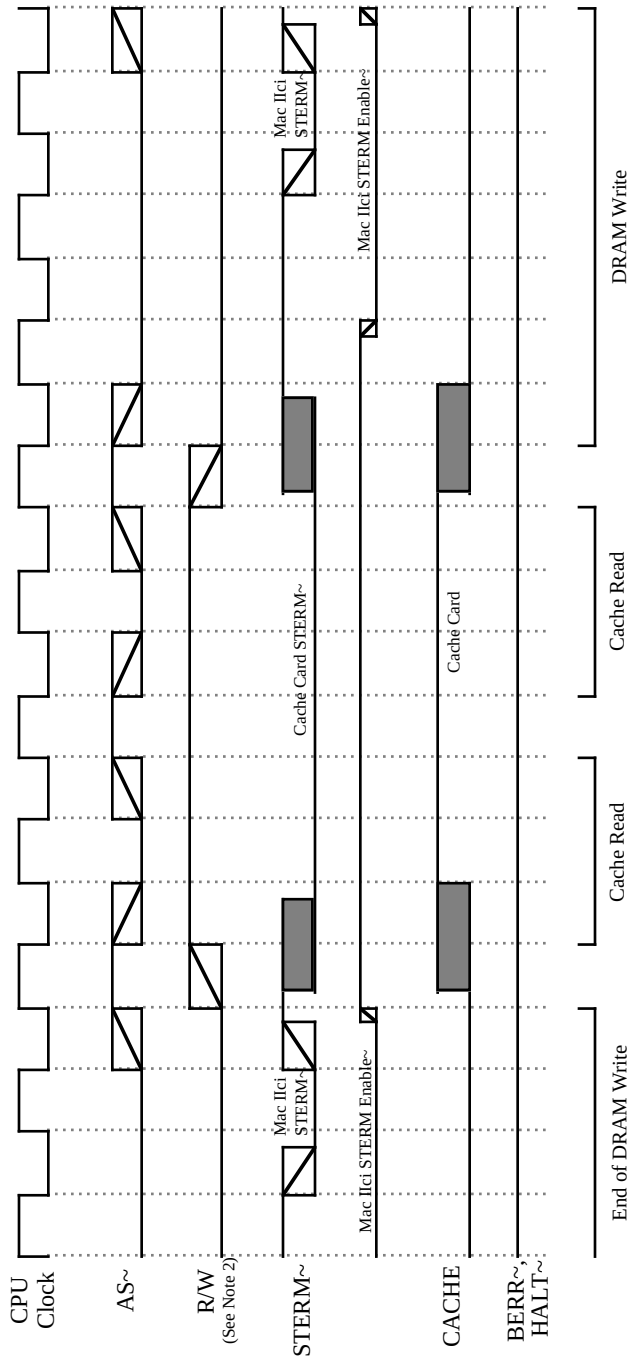
- **Figure C-3** Timing diagram showing the interaction between a generic cache card and the Macintosh IIci



Note1: The transitions indicated for cache card signals STERM~, CACHE, BERR~, and HALT show the range of acceptable transition times htat will allow the fastest possible operation of the computer and the cache. Transitions outside of these ranges may cause various sorts of errors or contention, or may delay the access that follows.

Note 2: A false parity error may occur after a cache card access if STERM~ is not driven high before the rising clock edge that follows the first falling edge after the CACHE signal is driven low.

- **Figure C-4** Timing diagram showing the interaction between a generic cache card's signals and the Macintosh IIci NuBus' signals



Note1: The transitions indicated for cache card signals STERM~, CACHE, BERR~, and HALT show the range of acceptable transition times htat will allow the fastest possible operation of the computer and the cache. Transitions outside of these ranges may cause various sorts of errors or contention, or may delay the access that follows.

Note 2: This timing diagram illustrates the effect of writes (R/W=0) on a cache card. The effect of cache-inhibited accesses (CIOUT~=0) and coprocessor accesses (FCO-2=111)_ follow similar timing. Figure B-5 is a complete pinout diagram and is provided only for use with emulators and testers.

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